

Quick Reference Guide for Thermal Design for Power Semiconductor SMD type: Part 2

Outline:

The Quick Reference Guide for Thermal Design for Power Semiconductor SMD type: Part 2 is designed to provide at-a-glance information as a supplement to other application notes on thermal design. Simplified models are used herein to make it easy to understand thermal tendencies. This document is a sequel to [Quick Reference Guide for Thermal Design for Power Semiconductor SMD type](#) available on the website of Toshiba Electronic Devices & Storage Corporation.

Table of Contents

Outline:.....	1
Table of Contents	2
0. Introduction: Quick Reference Guide for Thermal Design for Power Semiconductor SMD type: Part 2.....	3
0.1. Background	3
0.2. Summary	4
1. Board material vs. thermal resistance.....	6
2. TIM thickness vs. thermal resistance	7
3. Effects of a TIM vs. thermal resistance	8
4. Comparison of temperatures of thermally interfering chips	9
5. Effects of thermally interfering traces.....	10
6. Dense placement vs. dispersed placement.....	11
7. Orientation of a heatsink vs. thermal resistance	12
8. Length of thermal fins vs. thermal resistance.....	13
9. Thickness of thermal fins vs. thermal resistance.....	14
10. Number of thermal fins vs. thermal resistance	15
11. Distance between a heatsink and the inner wall of a chassis vs. thermal resistance.....	16
12. Distance between a device and the inner wall of a chassis vs. thermal resistance	17
13. Measure #1 for heat spots (high-thermal-conductivity sheet).....	18
14. Measure #2 for heat spots (casing material)	19
15. Air direction and velocity vs. thermal resistance.....	20
16. Effects of cooling air velocity and device placement (e.g., correlation between devices with high and low power dissipation)	21
17. Effects of cooling air velocity and device placement (e.g., correlation between physically large and small devices)	22
RESTRICTIONS ON PRODUCT USE	23

0. Introduction: Quick Reference Guide for Thermal Design for Power Semiconductor SMD type: Part 2

0.1. Background

Discrete semiconductor devices in automotive and high-power electronic applications (for power supply, motor drive, etc.) are increasingly exposed to higher temperatures because of 1) a reduction in system size, 2) an increase in board assembly density, and 3) an increase in system power consumption due to performance enhancement. It is therefore important to grasp the thermal profile of your system design in the early stages of development. Under these circumstances, Toshiba provides several application notes on its website to help you reduce chip temperature and thereby facilitate thermal design. Lately, Toshiba released [Hints and Tips for Thermal Design for Discrete Semiconductor Devices — Part 2](#) that provides the results of simulations using natural convection models and [Hints and Tips for Thermal Design for Discrete Semiconductor Devices — Part 3](#) that summarizes the results of simulations using forced-convection models that emulate real hardware conditions more closely.

Since these application notes were published, we have received feedback from their readers, indicating that they need a handy at-a-glance guide to know just enough about thermal design quickly. [The Quick Reference Guide for Thermal Design for Power Semiconductor SMD type](#) was created to provide at-a-glance information as a supplement to other application notes.

This document is a sequel to it. The surface-mount package models for power semiconductor devices used herein are based on SOP Advance and TO-220SM(W) for [Toshiba's MOSFETs](#).^{Note} These models are simplified to make it easy to grasp only thermal tendencies. While package models are simplified, a board model used as a baseline represents a 1.6 mm thick four-layer board with a trace thickness of 35 μm . This application note is in a question-and-answer format. We hope that it will help you understand thermal behavior.

Note: Toshiba's power semiconductor SMDs are available in a wide range of packages, including thermally enhanced DSOP Advance with a double-sided-cooling structure.

0.2. Summary

The following table summarizes the simulation results, indicating that each countermeasure provides a reduction in thermal resistance.

Contents	Countermeasure	Reduction in thermal resistance ^{Note1}
1. Board material vs. thermal resistance	Using a ceramic board to reduce thermal resistance considerably	FR4 ⇒ ceramic board: 56% reduction
2. TIM ^{Note2} (grease) thickness vs. thermal resistance	TIM that is just thick enough to fill a gap	1.0 mm ⇒ 0.1 mm: 6% reduction
3. Effects of a TIM vs. thermal resistance	Reducing a gap between two components and using a TIM to further reduce thermal resistance	20 μm gap ⇒ TIM insertion: 11% reduction
4. Comparison of thermally interfering chips	Reducing device-to-device spacing causes a rise in temperature because of the effect of thermal interference.	(Effect of thermal interference: Heating of a single chip ⇒ simultaneous heating of two chips: 41% increase in chip temperature)
5. Effects of thermally interfering traces	Thermal interference occurs, depending on the shapes of traces.	–
6. Dense placement vs. dispersed placement	Allowing as much spacing as possible when placing many heat-generating devices on a board	Dense placement ⇒ dispersed placement: 13% reduction
7. Orientation of a heatsink vs. thermal resistance	Orienting thermal fins vertically in the case of natural convection	Fins facing down ⇒ Fins standing vertically: 6% reduction
8. Length of thermal fins vs. thermal resistance	Increasing the length of fins (The reduction in thermal resistance levels off at a certain point as the length of fins is increased.)	0 mm ⇒ 15 mm: 29% reduction
9. Thickness of thermal fins vs. thermal resistance	Optimizing the thickness of thermal fins	0.2mm ⇒ 2.0mm: 4% reduction
10. Number of thermal fins vs. thermal resistance	Optimizing the number of thermal fins	3 fins ⇒ 9 fins: 16% reduction
11. Distance between a heatsink and the inner wall of a chassis vs. thermal resistance	Providing more spacing between a heatsink and the inner wall of a chassis	5 mm ⇒ 80 mm: 26% reduction
12. Distance between a device and the inner wall of a chassis vs. thermal resistance	Minimizing the gap between a device and the inner wall of a chassis and inserting a TIM between them	2 mm spacing ⇒ 0.1 mm gap filled by a TIM: 38% reduction
13. Measure #1 for heat spots (high-thermal-conductivity sheet)	Attaching a high-thermal-conductivity sheet inside a casing to diffuse heat across its surface	No sheet ⇒ Attaching a sheet: Up to 15% reduction in casing surface temperature
14. Measure #2 for heat spots (casing material)	Using a casing made of a material with high thermal conductivity (λ)	Low λ ⇒ high λ: Up to 19% reduction in casing surface temperature
15. Air direction and velocity vs. thermal resistance	Blowing air at high velocity in a direction parallel to thermal fins	Perpendicular ⇒ parallel: Up to 15%pp ^{Note3} reduction 0.1 m/s ⇒ 2.0 m/s: 41% reduction
16. Effects of cooling air velocity and device placement (e.g., correlation between	Air velocity and device-to-device spacing have greater effects on devices with lower power dissipation.	–

devices with high and low power dissipation)		
17. Effects of cooling air velocity and device placement (e.g., correlation between physically large and small devices)	Placing small devices upwind and large ones downwind to reduce overall temperature	–

Note 1: The reductions in thermal resistance shown above are the results under specific conditions. For details, see the following pages.

Note 2: TIM stands for thermal interface material and collectively refers to any material that is inserted between a heatsink and a device or between a heatsink and a board in order to enhance the thermal coupling between them.

Note 3: %pp (percentage point) represents an arithmetic difference between two percentages.

1. Board material vs. thermal resistance

Question: How much does the board material affect the thermal resistance?

Conditions:

Package: SOP Advance

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 2.0\text{ W}$

Board: Four-layer board (2 inches sq.), 1.6 mm thick

Vias: No via or nine vias below a device

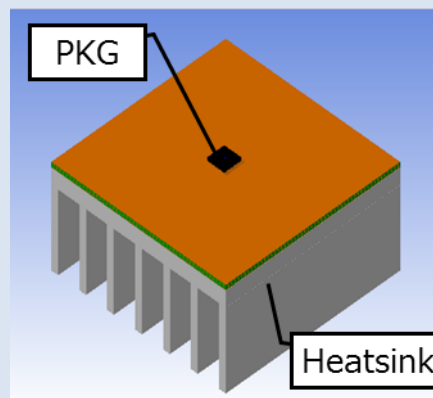
Board materials: Two types (FR4 and ceramic)

Thermal conductivity: FR4 = $0.35\text{ W/m}\cdot\text{K}$

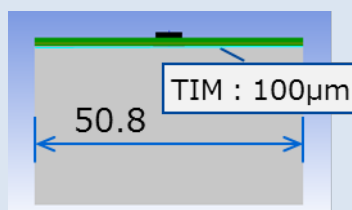
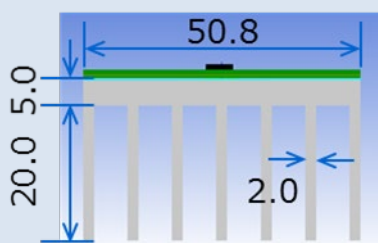
Ceramic = $15\text{ W/m}\cdot\text{K}$

TIM = $3.3\text{ W/m}\cdot\text{K}$ (grease)

Cu coverage: 100% (35 μm thick) on all layers



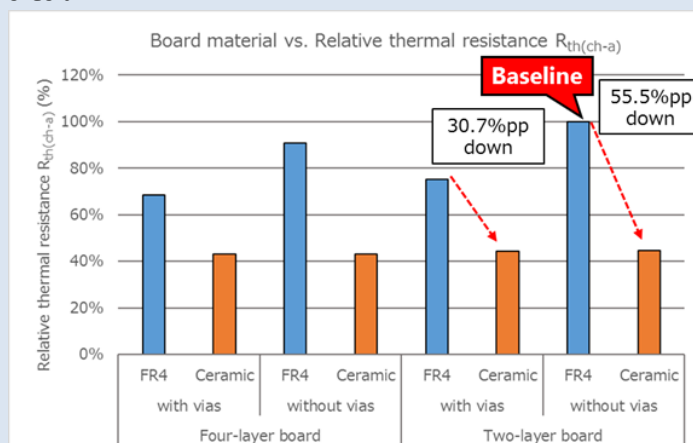
Unit in mm



Conclusion: Using a ceramic board results in lower thermal resistance than using an FR4 board. A ceramic board is particularly beneficial when the board has no vias.

Results: Using a ceramic board with high thermal conductivity helps reduce thermal resistance considerably. Using a ceramic board is particularly beneficial when vias cannot be drilled through a board. A ceramic board results in more than 50% lower thermal resistance than an FR4 board (FR4 $\Rightarrow$ ceramic: 55.5% reduction).

Data:



Board	Via	Board material	Relative thermal resistance
Four layer	Yes	FR4	68.5%
		Ceramic	43.2%
	No	FR4	90.9%
		Ceramic	43.2%
Two layer	Yes	FR4	75.2%
		Ceramic	44.5%
	No	FR4	100%
		Ceramic	44.5%

Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100\text{ (\%)}$

Note 2: Relative to a baseline model of a two-layer board with no via

2. TIM thickness vs. thermal resistance

Question: How much does the thickness of a TIM affect the thermal resistance?

Conditions:

Package: SOP Advance

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 2.0\text{ W}$

Forced air cooling: 1.0 m/s (See the right-hand figure.)

Thickness of the TIM: See the figure shown below (five variations).

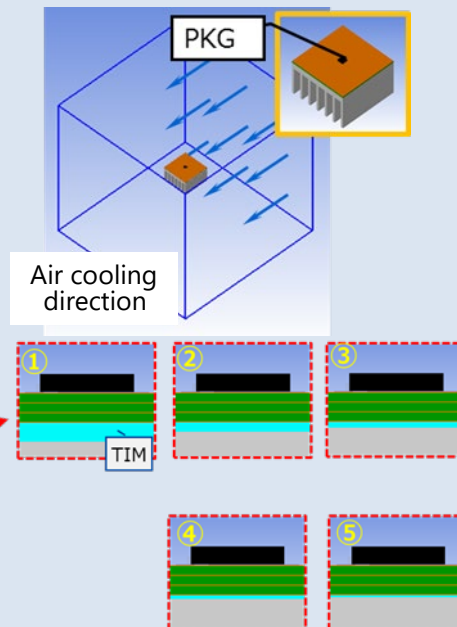
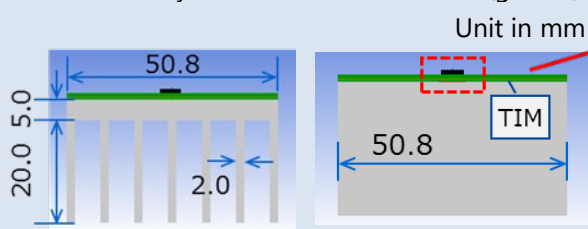
Board: Four-layer board (2 inches sq.), 1.6 mm thick

Board material: FR4

Cu coverage: 100% (35 μm thick) on all layers

Vias: Nine vias below a device

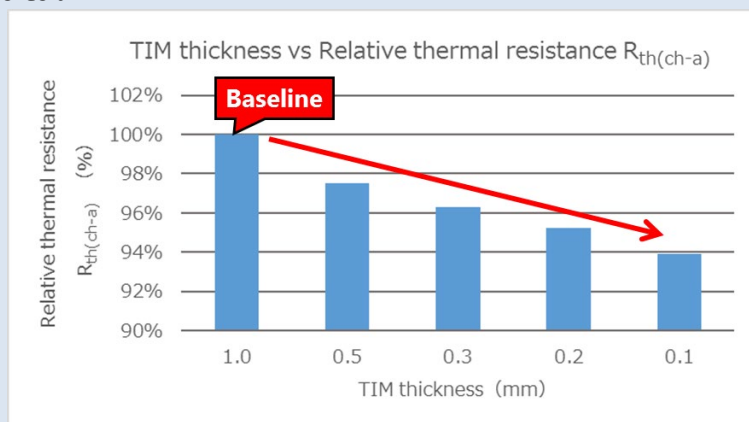
Thermal conductivity of the TIM = 1.2 W/m·K (grease)



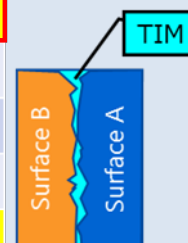
Conclusion: Use just enough TIM (grease) to fill a gap. An excessively thick TIM results in an increase in thermal resistance.

Results: Reducing the thickness of the TIM inserted between a board and a heatsink helps reduce thermal resistance (1.0 mm $\Rightarrow$ 0.1 mm: 6.1% reduction). Since the TIM has a thermal conductivity on the order of a fraction of one watt per m·K to several watts per m·K, an excessively thick TIM has an adverse effect. It is therefore desirable to fill only the gap between a board and a heatsink as shown above.

Data:



No.	TIM thickness (mm)	Relative thermal resistance
①	1.0	100%
②	0.5	97.5%
③	0.3	96.3%
④	0.2	95.2%
⑤	0.1	93.9%



Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100$ (%)

Note 2: Relative to a TIM with a thickness of 1.0 mm (①)

3. Effects of a TIM vs. thermal resistance

Question: How much does the insertion of a TIM affect the thermal resistance?

Conditions:

Package: SOP Advance

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 2.0\text{ W}$

Forced air cooling: 1.0 m/s (See the right-hand figure.)

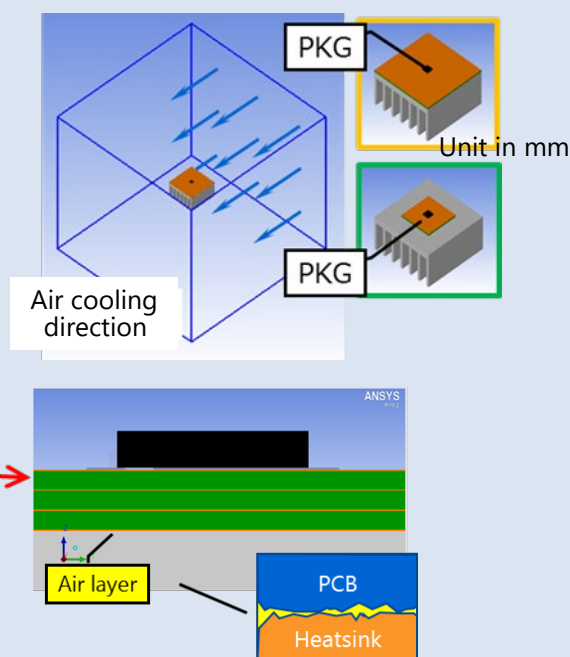
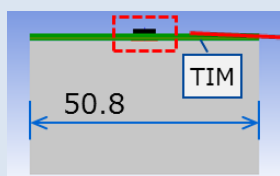
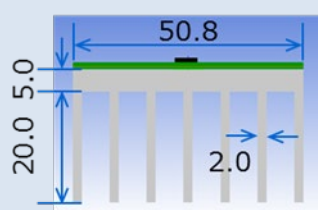
Thickness of an air layer: See the table below.

Boards: Four-layer boards (2 inches sq., 1 inch sq.), 1.6 mm thick

Cu coverage: 100% (35 μm thick) on all layers

Vias: Nine vias below a device

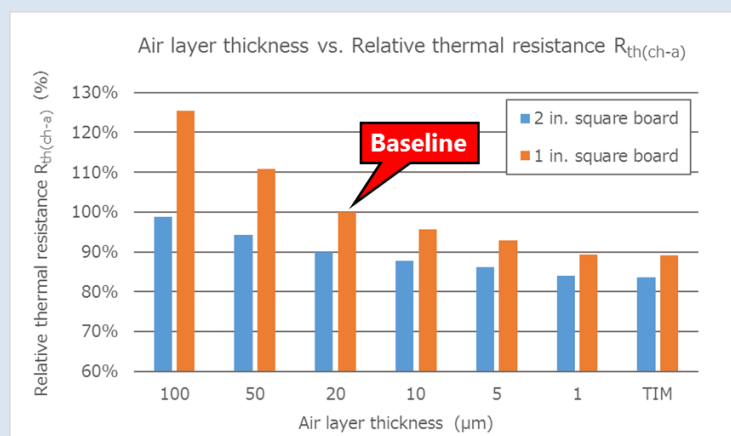
TIM: 100- μm thick;



Conclusion: Minimize a gap between two components to reduce thermal resistance. Using a TIM helps reduce thermal resistance further.

Results: When two solid components are in contact with each other, contact thermal resistance occurs because of an uneven interface. The thicker the air layer, the higher the contact thermal resistance and therefore the total thermal resistance. Inserting a TIM helps reduce thermal resistance (20 μm air layer $\Rightarrow$ TIM: 10.8% reduction). The smaller the contact area, the bigger the benefit a TIM provides.

Data:



Air layer thickness (μm)	Relative thermal resistance	
	2in. square	1in. square
100	98.9%	125%
50	94.2%	111%
20	89.9%	100%
10	87.7%	95.6%
5	86.1%	92.8%
1	83.9%	89.4%
TIM	83.7%	89.2%

Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100\%$

Note 2: Relative to a baseline model with a board one inch square and an air layer with a thickness of 20 μm

4. Comparison of temperatures of thermally interfering chips

Question: How much does thermal interference affect chip temperature?

Conditions:

Package: SOP Advance

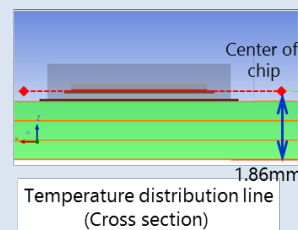
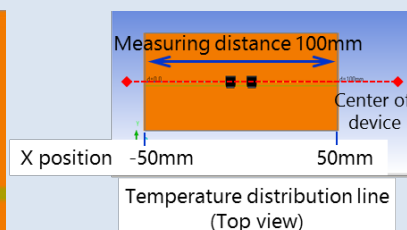
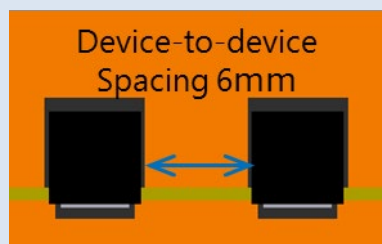
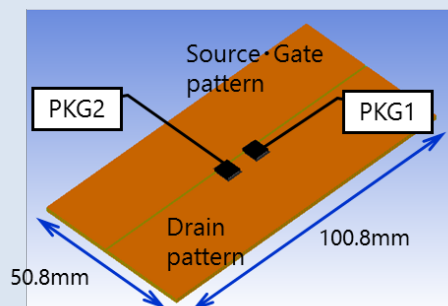
Conditions: $T_a = 25^\circ\text{C}$, $P_D = 2.0\text{ W}$ per device

Board: Four-layer board (4 × 2 inches)

Thickness: 1.6 mm

Cu coverage: 100% (35 μm thick) on all layers

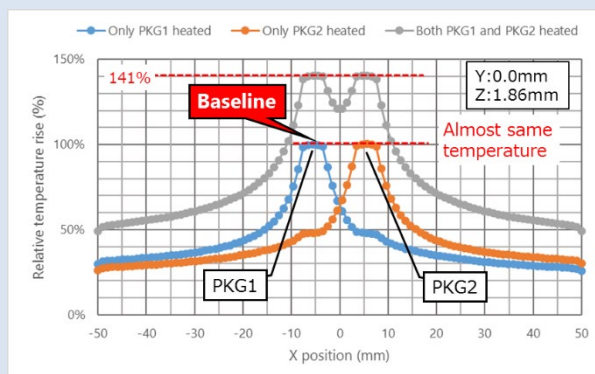
The drain is separated from the source and the gate only on the surface layer.



Conclusion: When two nearby devices generate heat simultaneously, thermal interference causes their chip temperature to rise more than in the case that only one device generates heat.

Results: Two devices are placed side by side and heated separately and simultaneously. Even at the same power dissipation, heating two devices simultaneously results in a chip temperature 41% higher than heating them separately. This difference occurs because when two devices are heated simultaneously, they thermally interfere with each other, causing the temperature of each device to rise further. It is therefore necessary to provide sufficient spacing between two devices.

Data:



PKG1 P_D (W)	PKG2 P_D (W)	Relative temperature rise	
		PKG1	PKG2
2.0	0	100%	48.1%
0	2.0	47.8%	100%
2.0	2.0	141%	141%

Note 1: Relative temperature rise in the X direction = temperature rise_at_each_position / baseline_temperature_rise × 100 (%)

Note 2: The baseline is the maximum rise in chip temperature that occurs when only PKG1 is active.

Note 3: The sum of the rises in chip temperature in PKG1 and PKG2 that occur in the X direction when they are separately heated is almost equal to the rise in chip temperature that occurs when they are simultaneously heated.

5. Effects of thermally interfering traces

Question: How much do the shapes of Cu traces affect the device temperature?

Conditions:

Package: Six devices housed in SOP

Advance

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 0.5\text{ W}$ per device

Board: Four-layer board (2 inches sq.)

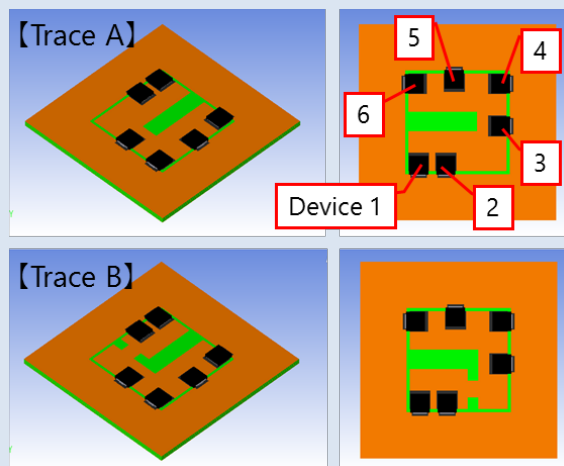
Thickness: 1.6 mm

Traces: Top layer = A and B

Layers 2, 3 and 4 = Cu covered

35 μm thick on all layers

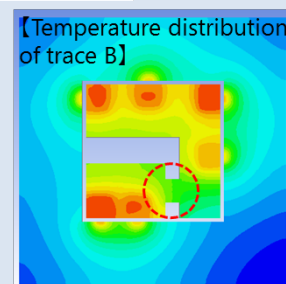
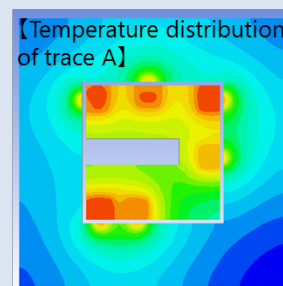
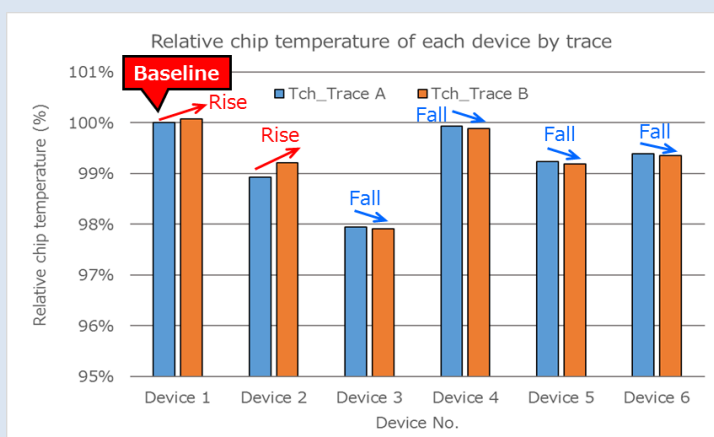
Placement: The six devices are placed in such a manner that their E-pads are on top of the trace at the center of the board. (See the right-hand figure for trace and device placement.)



Conclusion: The impact of thermal interference depends on the shapes of traces.

Results: Since the width of Trace B is narrow at the position highlighted by the red circle, it hampers the flow of heat from Devices 1 and 2 to the other devices. In addition, Devices 1 and 2 suffer from thermal interference that occurred inside small traces. The temperature of Device 2, in particular, becomes higher than that of Trace A.

Data:



Note 1: Relative chip temperature T_{ch}

= $\text{chip_temperature_of_each_device} / \text{baseline_temperature} \times 100 (\%)$

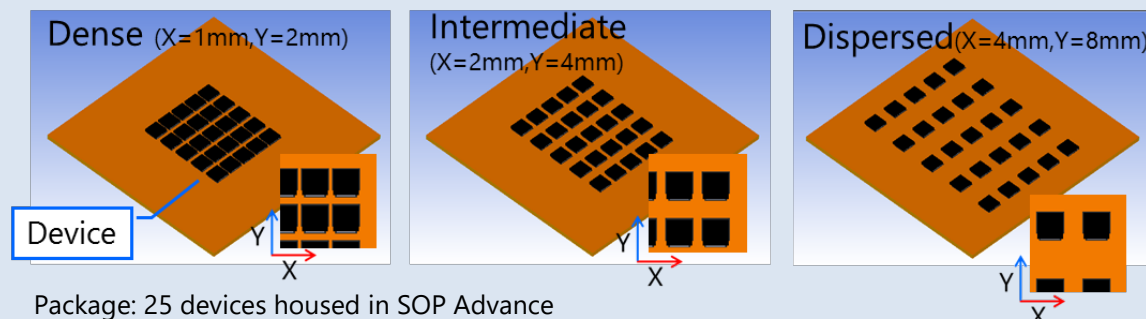
Note 2: Relative to the chip temperature of Device 1 on a board with Trace A

Note 3: In the case of both Trace A and Trace B, the temperatures of three devices (1, 4, and 6) at the corners become high, indicating that they do not dissipate heat efficiently.

6. Dense placement vs. dispersed placement

Question: How much does device placement affect the thermal resistance?

Conditions:



Package: 25 devices housed in SOP Advance

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 0.2\text{ W}$ per device

Board: Four-layer board (3 inches sq.), 1.6 mm thick

Board material: FR4

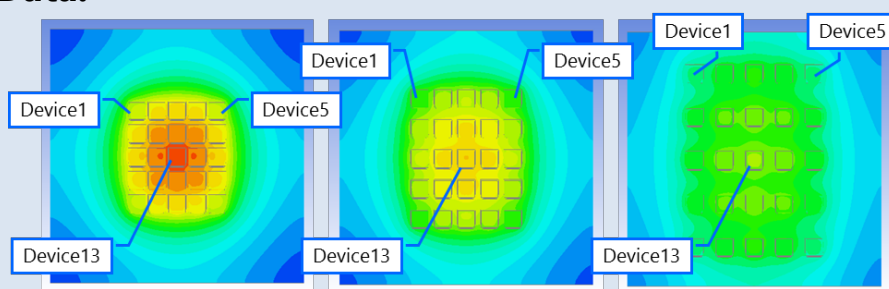
Cu coverage: 100% (35 μm thick) on all layers

Device placement: Dense, intermediate, and dispersed (See the above figure.)

Conclusion: Thermal resistance can be reduced by providing sufficient spacing between heat sources on a board.

Results: When a board is densely populated with devices, their temperatures and thermal resistances increase. The temperature at the center of these devices tends to increase considerably, causing thermal resistance to increase. Temperature decreases toward the edge of the board, causing thermal resistance to decrease as well (Dense placement $\Rightarrow$ dispersed placement: 12.7% reduction). If a board has many heat sources, it is desirable to provide sufficient spacing between them.

Data:



Temperature distribution viewed from above the model

(comparison in the same temperature range)

Note 1: Relative thermal resistance = $\frac{\text{thermal_resistance_of_each_device}}{\text{baseline_thermal_resistance}} \times 100 (\%)$

Note 2: Relative to the maximum thermal resistance out of 25 devices in a dense placement model

Note 3: The minimum and the maximum temperature numbers are ones with the minimum and the maximum thermal resistances among 25 devices of each placement model.

Note 4: The X and Y values are mold-to-mold spacing in the X and Y directions.

Device placement	Device No. and Relative thermal resistance			
	Min. No & ratio		Max. No & ratio	
Dense	1	88.3%	13	100%
Intermediate	1	83.6%	13	94.7%
Dispersed	1,5	79.1%	13	87.3%

7. Orientation of a heatsink vs. thermal resistance

Question: How much does the orientation of a heatsink affect the thermal resistance?

Conditions:

Package: SOP Advance

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 2.0\text{ W}$

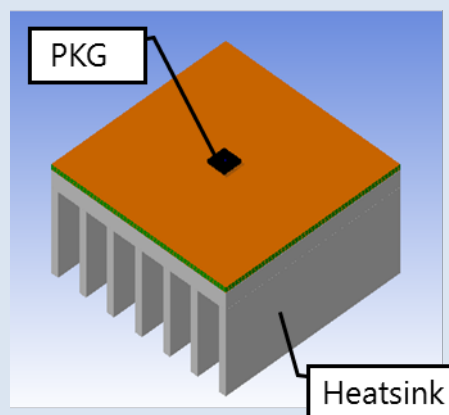
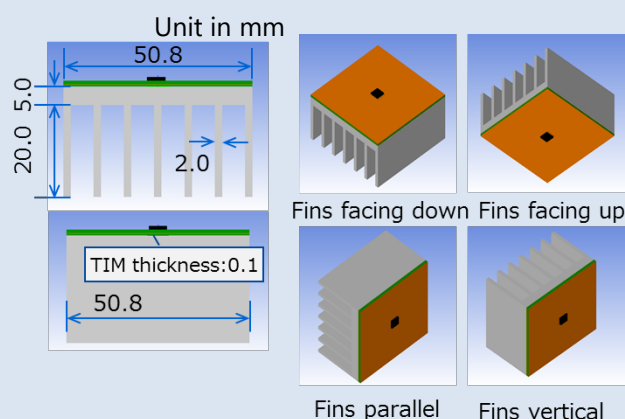
Orientations of the heatsink: See the figure below.

Board: Four-layer board (2 inches sq.), 1.6 mm thick

Board material: FR4

Cu coverage: 100% (35 μm thick) on all layers

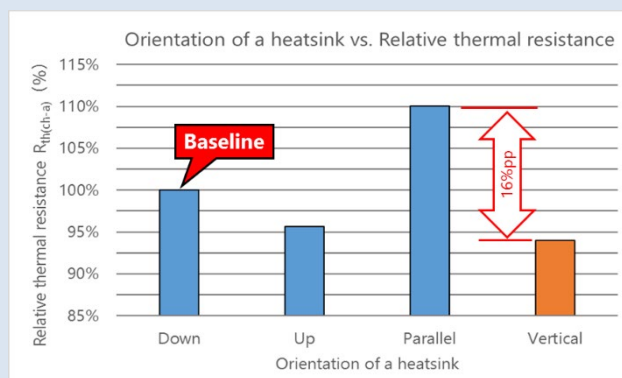
Vias: 9 vias below a device



Conclusion: In natural convection, thermal resistance depends on the orientation of thermal fins. It is desirable to attach a heatsink with its thermal fins standing vertically.

Results: In the case of natural convection, thermal resistance depends on the orientation of thermal fins. When air flows smoothly along the surfaces of the fins, heat disperses rapidly, causing thermal resistance to decrease (Fins facing down $\Rightarrow$ Fins standing vertically: 6% reduction). Note that there is a difference of 16%pp between the minimum and maximum thermal resistances.

Data:



Fins orientation	Relative thermal resistance
Down	100%
Up	95.7%
Parallel	110%
Vertical	94.0%

Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100$ (%)

Note 2: Relative to a baseline model with thermal fins facing down

8. Length of thermal fins vs. thermal resistance

Question: How much does the length of thermal fins affect the thermal resistance?

Conditions:

Package: TO-220SM(W)

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 7.0\text{ W}$

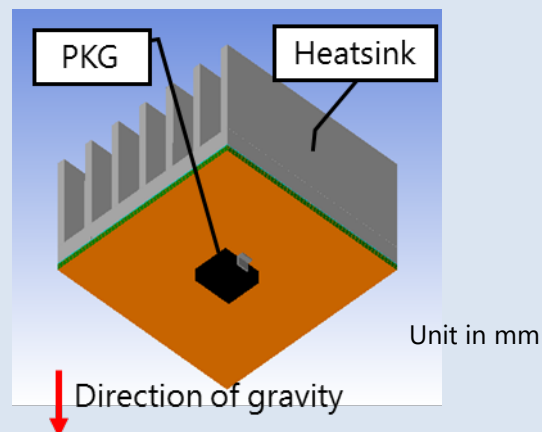
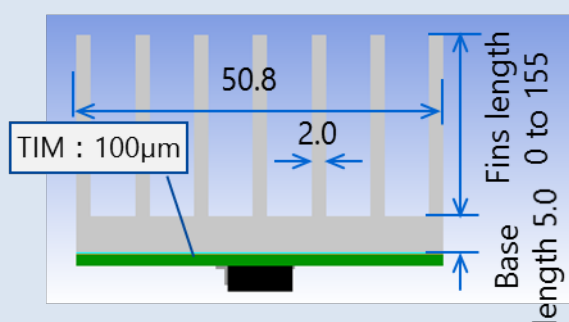
Board: Four-layer board (2 inches sq.), 1.6 mm thick

Cu coverage: 100% (35 μm thick) on all layers

Vias: 25 vias below a device

Heatsink: Seven fins with a thickness of 2.0 mm

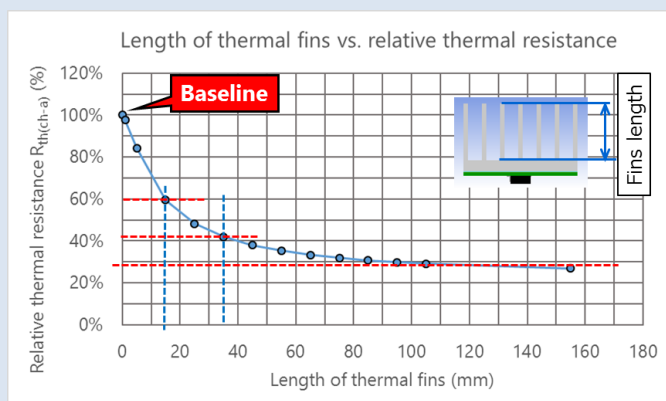
See the following table for the length of fins.



Conclusion: Thermal resistance can be reduced by increasing the length of thermal fins. However, it levels off at a certain point.

Results: Thermal resistance can be reduced by increasing the length of thermal fins. In the case of the model shown above, a heatsink with 15 mm thermal fins provides a 28.6% reduction in thermal resistance. This is considered to be the effects of an increase in the total surface area of the fins and the overall envelope volume of the heatsink. Note that, however, thermal resistance does not decrease linearly with the fin length and levels off at a certain point.

Data:



Fins length (mm)	Relative thermal resistance	Fins length (mm)	Relative thermal resistance
0	100%	55	54.3%
1	98.8%	65	52.9%
5	89.1%	75	51.9%
15	71.4%	85	51.0%
25	63.4%	95	50.4%
35	58.9%	105	49.9%
45	56.2%	155	48.2%

Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100$ (%)

Note 2: Relative to a heatsink having only a base (with a thickness of 5.0 mm) and no fin.

9. Thickness of thermal fins vs. thermal resistance

Question: How much does the thickness of thermal fins affect the thermal resistance?

Conditions:

Package: TO-220SM(W)

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 7.0\text{ W}$

Board: Four-layer board (2 inches sq.), 1.6 mm thick

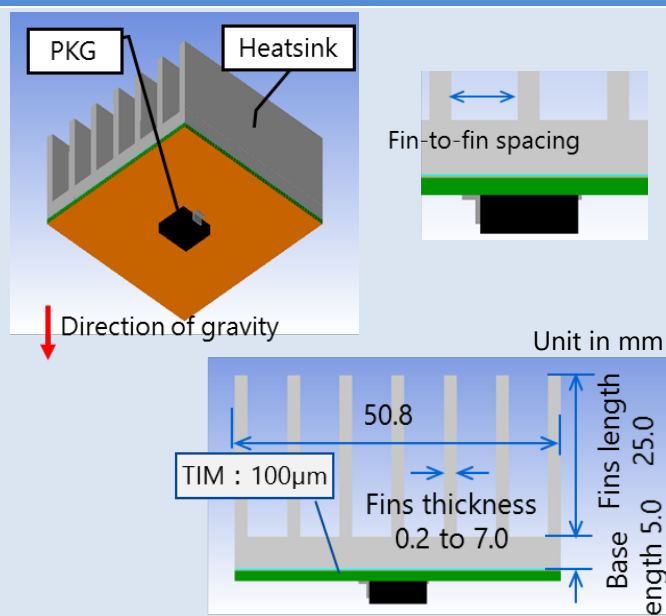
Board material: FR4

Cu coverage: 100% (35 μm thick) on all layers

Vias: 25 vias below a device

Heatsink: Seven fins with a length of 25.0 mm

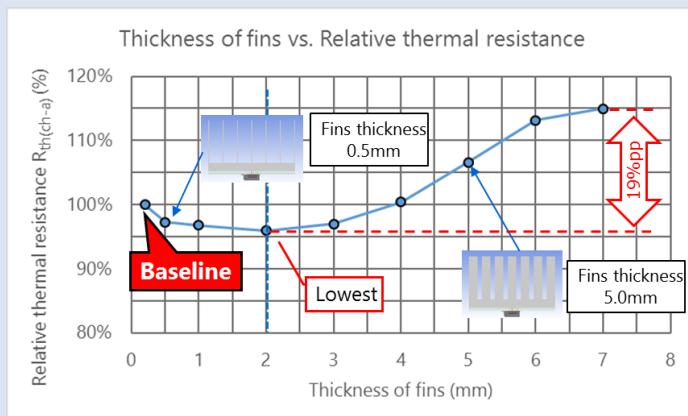
See the following table for the thickness of fins.



Conclusion: The optimal fin thickness varies regardless of the external dimensions and the number of thermal fins of the heatsink.

Results: The bellow figure shows the relationship between thermal resistance and fin thickness. The thermal resistance becomes the minimum when the fin thickness is 2.0 mm (0.2 mm $\Rightarrow$ 2.0 mm: 4% reduction). However, thermal resistance increases as the fin thickness is increased beyond this point. It is considered that as the fin thickness is increased, the fin-to-fin spacing decreases, causing air not to flow smoothly and therefore resulting in an increase in thermal resistance (difference between the minimum and maximum thermal resistances: 19% points). Conversely, excessively thin fins cause heat dissipation from the fins to decrease, causing thermal resistance to increase. Therefore, fins with an optimal thickness should be selected.

Data:



Fins thickness (mm)	Fin-to-fin spacing (mm)	Relative thermal resistance
0.2	8.2	100%
0.5	7.9	97.3%
1.0	7.3	96.8%
2.0	6.1	96.0%
3.0	5.0	97.0%
4.0	3.8	100%
5.0	2.6	107%
6.0	1.5	113%
7.0	0.3	115%

Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100 (\%)$

Note 2: Relative to a baseline model with a fin thickness of 0.2 mm

10. Number of thermal fins vs. thermal resistance

Question: How much does the number of thermal fins affect the thermal resistance?

Conditions:

Package: TO-220SM(W)

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 7.0\text{ W}$

Board: Four-layer board (2 inches sq.), 1.6 mm thick

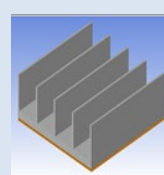
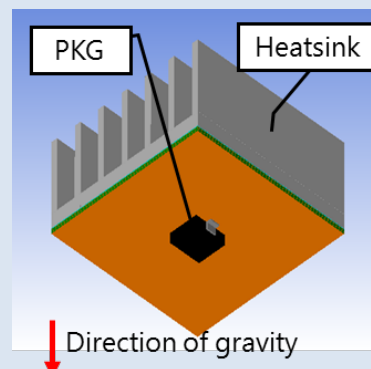
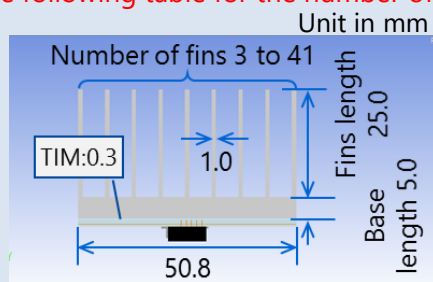
Board material: FR4

Cu coverage: 100% (35 μm thick) on all layers

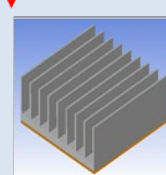
Vias: 25 vias below a device

Heatsink: Fins with a thickness of 1.0 mm and a length of 25.0 mm

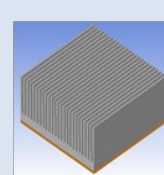
See the following table for the number of fins.



5 fins



9 fins

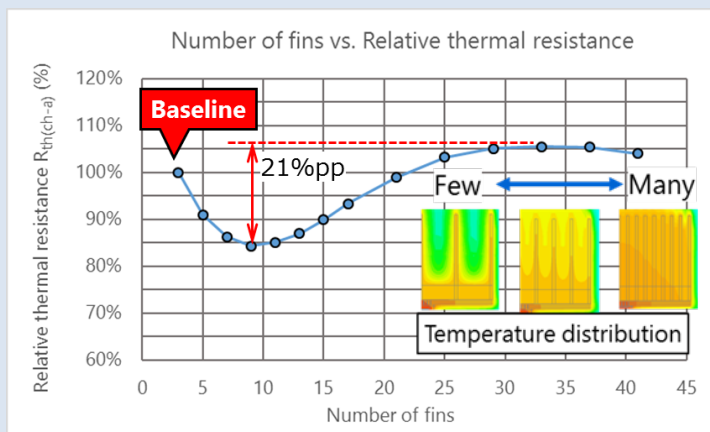


25 fins

Conclusion: The optimal fin count varies regardless of the external dimensions and the fin thickness of the heatsink.

Results: The below graph shows the thermal resistance of a device having different numbers of thermal fins with the same thickness. A heatsink with nine fins provides the minimum thermal resistance (3 fins $\Rightarrow$ 9 fins: 15.7% reduction). A heatsink with more fins provides less space where air flows. Therefore, its cooling effect levels off at a certain fin count, causing thermal resistance to increase (difference between minimum and maximum thermal resistances: 21% points). Conversely, a heatsink with too few thermal fins does not provide sufficient heat dissipation because of a low surface area, causing thermal resistance to increase.

Data:



Number of fins	Relative thermal resistance	Number of fins	Relative thermal resistance
3	100%	17	93.3%
5	90.9%	21	98.9%
7	86.3%	25	103%
9	84.3%	29	105%
11	85.0%	33	106%
13	87.0%	37	105%
15	89.9%	41	104%

Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100 (\%)$

Note 2: Relative to a baseline model of a heatsink with three fins

11. Distance between a heatsink and the inner wall of a chassis vs. thermal resistance

Question: How much does the distance between a heatsink and a chassis affect the thermal resistance?

Conditions:

Package: TO-220SM(W)

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 5.0\text{ W}$

Board: Four-layer board (2 inches sq.), 1.6 mm thick

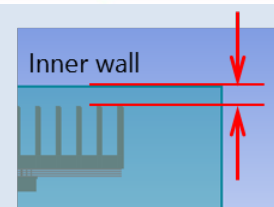
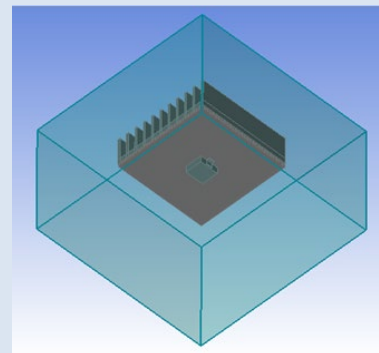
Cu coverage: 100% (35 μm thick) on all layers

Vias: 25 vias below a device

Heatsink: 50.0×51.5 mm, 11 fins

Chassis: 100×100 mm, arbitrary height, aluminum

Heatsink-to-chassis distance: See the table below.

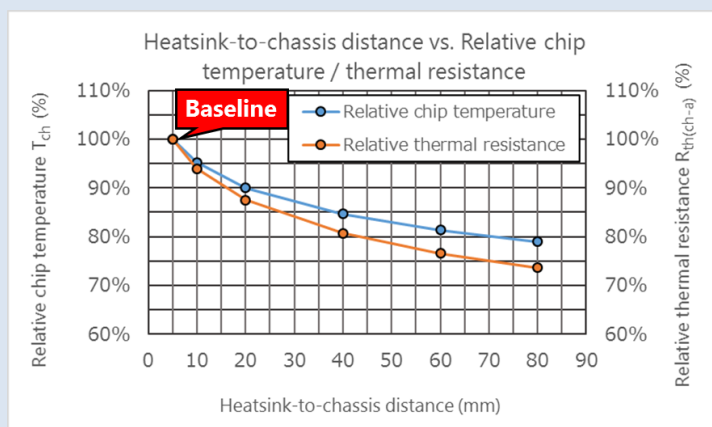


Heatsink-to-chassis distance

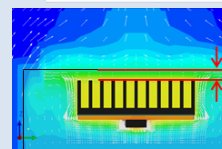
Conclusion: Chip temperature and thermal resistance decrease as the distance between a heatsink and a chassis increases.

Results: When placing a heatsink inside a chassis, thermal resistance can be reduced by providing as much spacing as possible between the heatsink and the chassis (5 mm $\Rightarrow$ 80 mm: 26.4% reduction). This is because, with more spacing, natural convection has a greater cooling effect.

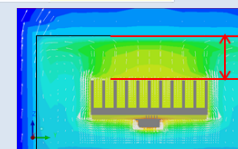
Data:



Heatsink-to-chassis distance (mm)	Relative chip temperature	Relative thermal resistance
5	100%	100%
10	95.2%	94.0%
20	90.0%	87.5%
40	84.6%	80.7%
60	81.3%	76.6%
80	79.0%	73.6%



Distance 5mm



Distance 20mm

Note 1: Relative chip temperature = $\text{each_chip_temperature} / \text{chip_temperature_of_baseline_model} \times 100$ (%)

Note 2: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100$ (%)

Note 3: Relative to a baseline model with an X distance of 5 mm

12. Distance between a device and the inner wall of a chassis vs. thermal resistance

Question: How do the distance between a device and a chassis and the insertion of a TIM affect thermal resistance?

Conditions:

Package: TO-220SM(W)

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 2.0\text{ W}$

Board: Four-layer board (2 inches sq.),
1.6 mm thick

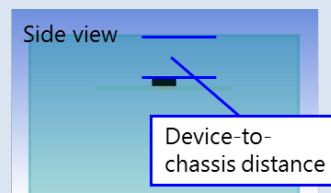
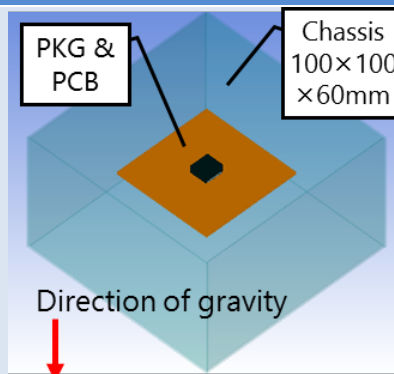
Cu coverage: 100% (35 μm thick) on all layers

Vias: 25 vias below a device

Chassis: 100×100 mm, 1 mm thick, aluminum

Device-to-chassis distance: See the table below.

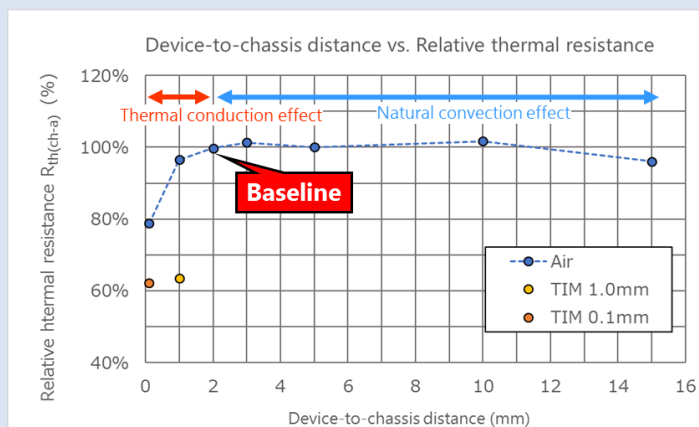
TIM (High-thermal-conductivity sheet): Surface thermal conductivity = 700 $\text{W/m}\cdot\text{K}$, vertical = 10 $\text{W/m}\cdot\text{K}$



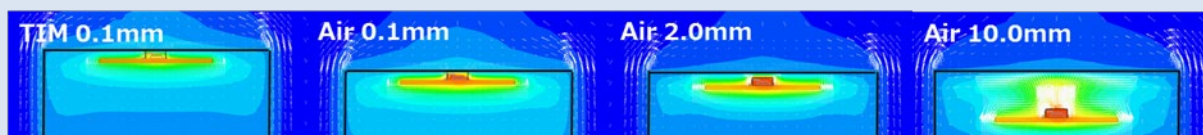
Conclusion: It is desirable to minimize the distance between a device and a chassis. Inserting a TIM between a device and a chassis helps reduce thermal resistance considerably.

Results: Thermal resistance decreases as the device-to-chassis distance decreases. When the device-to-chassis distance is 2 mm or less, thermal conduction becomes dominant as air does not flow smoothly through this spacing. With a greater device-to-chassis distance, natural convection begins to have a positive effect. In addition, thermal resistance can be reduced considerably by inserting a TIM between a device and a chassis (2 mm spacing $\Rightarrow$ 0.1 mm spacing filled by TIM: 38% reduction).

Data:



Device-to-chassis distance (mm)	Relative thermal resistance	Note
0.1	78.8%	Air
1.0	96.5%	Air
2.0	100%	Air
3.0	101%	Air
5.0	100%	Air
10.0	102%	Air
15.0	96.0%	Air
1.0	63.6%	TIM
0.1	62.1%	TIM



Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100 (\%)$

Note 2: Relative to a baseline model with a device-to-chassis distance of 2.0 mm

13. Measure #1 for heat spots (high-thermal-conductivity sheet)

Question: How can I reduce heat spots on the surface of a casing?

Conditions:

Package: Five devices housed in SOP Advance

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 1\text{ W}$ per device

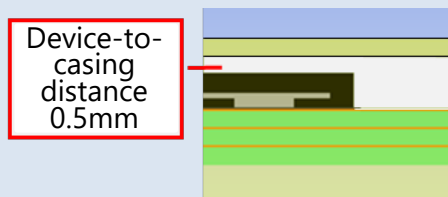
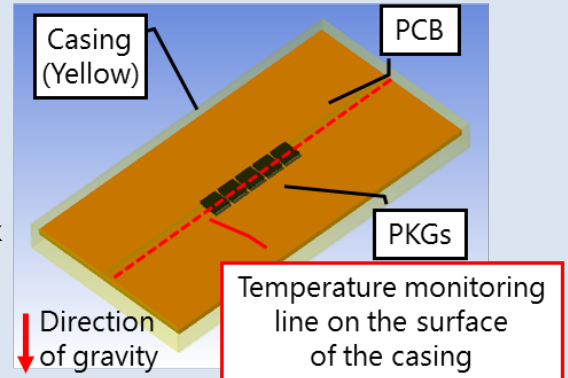
Board: Four-layer board (97 × 48.8 mm), 1.6 mm thick

Cu coverage: 100% (35 μm thick) on all layers

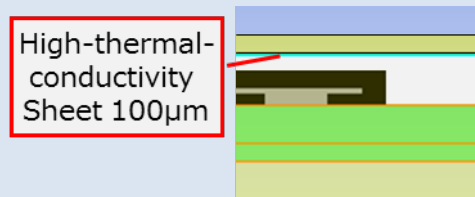
External casing dimensions: 100×50×8 mm, 0.5 mm thick

TIM (High-thermal-conductivity sheet): Surface thermal conductivity = 700 W/m·K

Thickness direction = 10 W/m·K



Model 1: Without a high-thermal-conductivity sheet

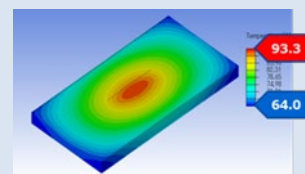
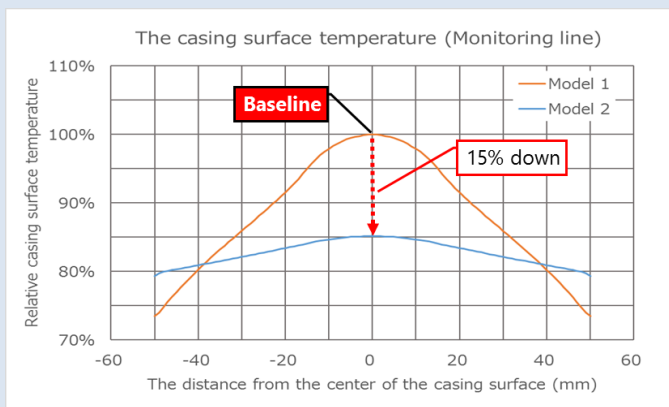


Model 2: With a high-thermal-conductivity sheet

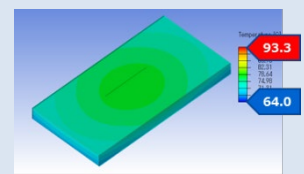
Conclusion: Attaching a high-thermal-conductivity sheet inside the casing helps reduce heat spots.

Results: If a heat source is housed in a thin casing, heat spots might occur on the surface of the casing. In this case, attaching a high-thermal-conductivity sheet inside the casing helps increase heat dissipation and thus reduce heat spots (No sheet $\Rightarrow$ Attaching a sheet: Up to 15% reduction in casing surface temperature).

Data:



Model 1: Without a high-thermal-conductivity sheet



Model 2: With a high-thermal-conductivity sheet

Note 1: Relative casing surface temperature = temperature_at_each_position / baseline_temperature × 100 (%)

Note 2: Relative to the baseline temperature at the center (0 mm position) of the casing surface without a high-thermal-conductivity sheet

14. Measure #2 for heat spots (casing material)

Question: How can I reduce heat spots on the surface of a casing?

Conditions:

Package: Five devices housed in SOP Advance

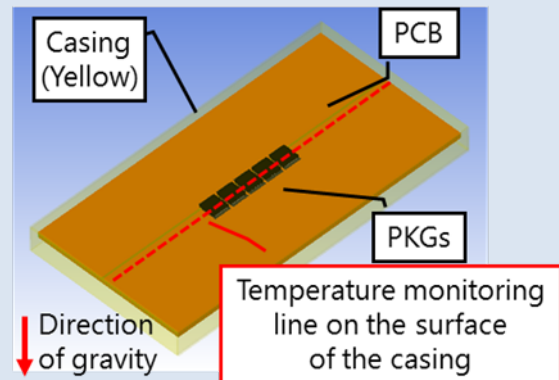
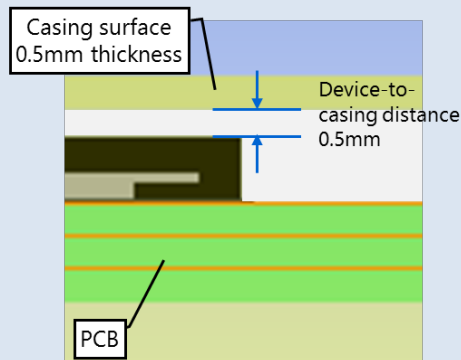
Conditions: $T_a = 25^\circ\text{C}$, $P_D = 1\text{ W}$ per device

Board: Four-layer board ($97 \times 48.8\text{ mm}$), 1.6 mm thick

Cu coverage: 100% ($35\text{ }\mu\text{m}$ thick) on all layers

External casing dimensions: $100 \times 50 \times 8\text{ mm}$, 0.5 mm thick

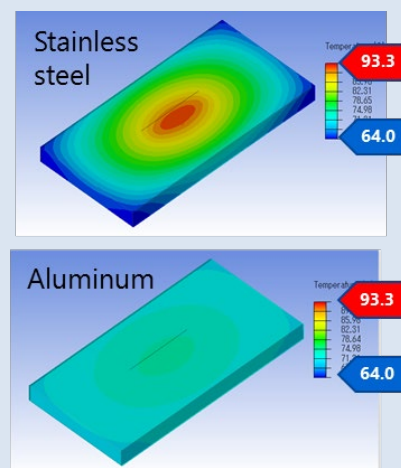
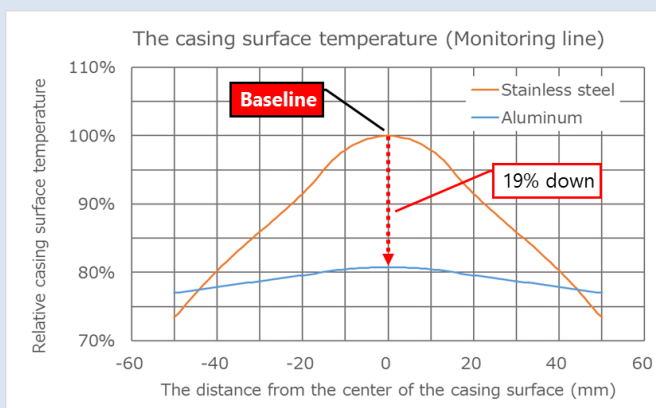
Casing materials: Stainless steel, aluminum



Conclusion: Using a high- λ material for the casing helps reduce heat spots.

Results: When a casing made of a material with low thermal conductivity is used, heat spots tend to occur on the surface of the casing. In contrast, using a casing with a high thermal conductivity helps reduce heat spots (Low $\lambda \Rightarrow$ high λ : Up to 19% reduction in casing surface temperature).

Data:



Note 1: Relative casing surface temperature

= $\text{temperature_at_each_position} / \text{baseline_temperature} \times 100 (\%)$

Note 2: Relative to the temperature at the center (0 mm position) of a stainless steel casing

15. Air direction and velocity vs. thermal resistance

Question: How much do the air direction and velocity relative to the thermal fins of a heatsink affect the thermal resistance?

Conditions:

Package: TO-220SM(W)

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 10.0\text{ W}$

Board: Four-layer board (2 inches sq.), 1.6 mm thick

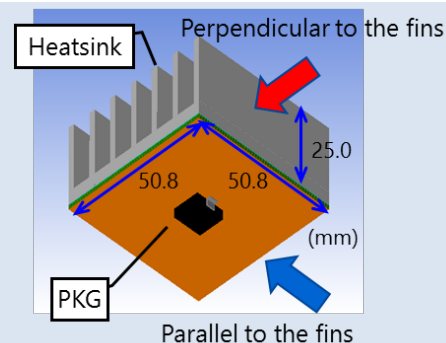
Cu coverage: 100% (35 μm thick) on all layers

Vias: 25 vias below a device

Heatsink: Seven fins, fin thickness = 2.0 mm, fin length = 25.0 mm, base =

5.0 mm, TIM

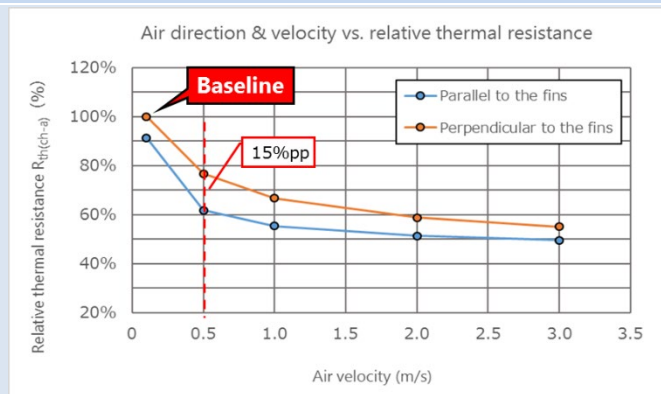
Air direction: Parallel and perpendicular to the thermal fins of a heatsink



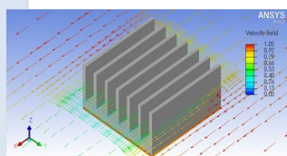
Conclusion: It is advisable to orient thermal fins in a direction parallel to the air flow. Thermal resistance decreases as air velocity increases, but levels off at a certain point.

Results: The below graph shows relative thermal resistances when air is blown toward the thermal fins of a heatsink in both parallel and perpendicular directions while changing air velocity. Blowing air to thermal fins in the parallel direction provides an up to 15% lower thermal resistance than blowing air in the perpendicular direction. Increasing air velocity provides a considerable reduction in thermal resistance (0.1 m/s $\Rightarrow$ 2.0 m/s: 41% reduction). However, the reduction levels off when air velocity reaches a certain point (2 m/s in the case of this model). It is considered that, at this point, the effect of air has spread across the entire surface of the fins.

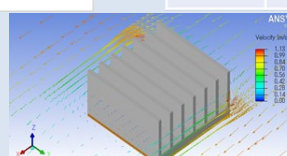
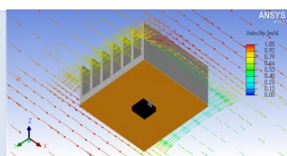
Data:



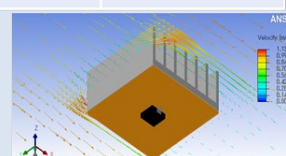
Air velocity (m/s)	Relative thermal resistance	
	Parallel to the fins	Perpendicular to the fins
0.1	91%	100%
0.5	62%	77%
1.0	55%	67%
2.0	51%	59%
3.0	50%	55%



Airflow: Parallel to the fins



Airflow: Perpendicular to the fins



Note 1: Relative thermal resistance $R_{th(ch-a)} = \text{each_thermal_resistance} / \text{baseline_thermal_resistance} \times 100 (\%)$

Note 2: Relative to a baseline model with an air velocity of 0.1 m/s blowing in a direction perpendicular to the thermal fins

16. Effects of cooling air velocity and device placement (e.g., correlation between devices with high and low power dissipation)

Question: How much does the placement of devices with high and low power dissipation (P_D) affect their thermal resistance?

Conditions:

Package: SOP Advance (one high- P_D device and one low- P_D device)

Conditions: $T_a = 25^\circ\text{C}$, $P_D = 5.0\text{ W}$ (high P_D), 0.5 W (low P_D), forced

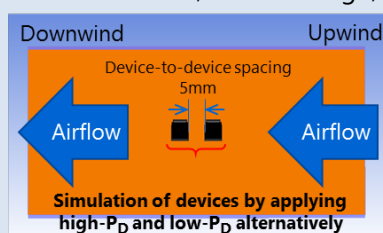
air cooling (air velocity: 1, 3, and 5 m/s)

Device-to-device spacing: See the figures below.

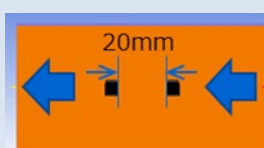
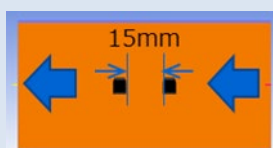
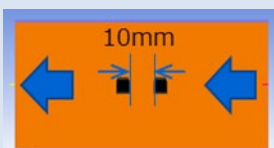
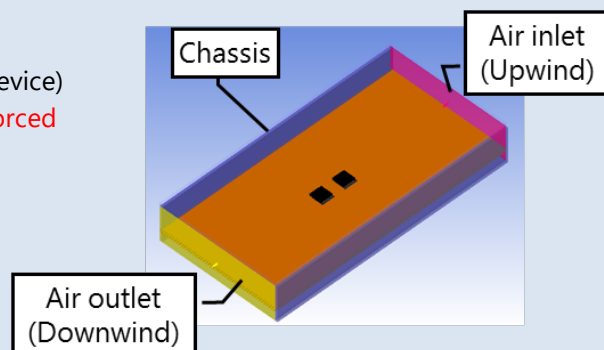
Board: Four-layer board (2×1 inches), 1.6 mm thick

Cu coverage: 100% ($35\text{ }\mu\text{m}$ thick) on all layers

Chassis: $101.6 \times 51.8\text{ mm}$, 15.6 mm high, 1.0 mm thick



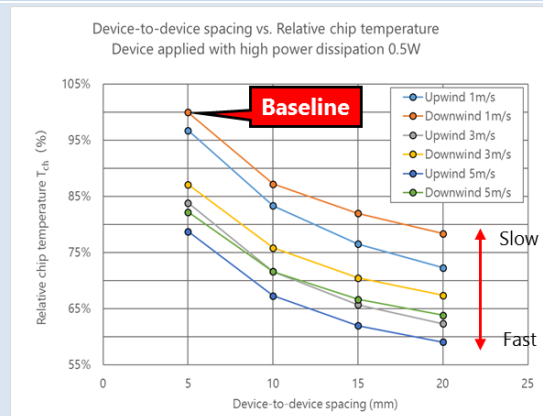
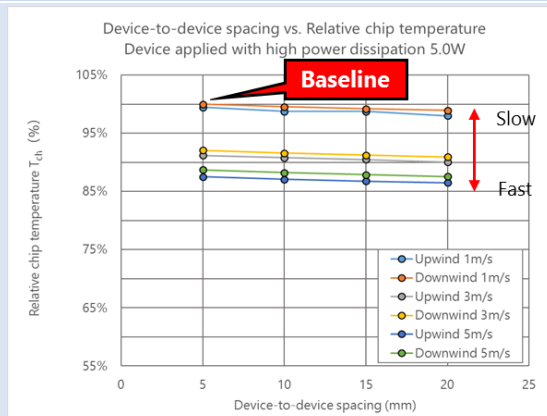
Top view (The top surface is not shown)



Conclusion: Air velocity and device-to-device spacing have greater effects on devices with lower power dissipation.

Results: The chip temperature of the low- P_D device depends on air velocity and device-to-device spacing. Also, the chip temperature of the device placed downwind tends to become higher than that of the device placed upwind. Air velocity has a greater impact on the chip temperature of the device placed downwind. In contrast, in the case of the high- P_D device, the chip temperature decreases as air velocity increases and does not depend greatly on device-to-device spacing. The device placed downwind exhibits chip temperature only slightly higher than that of the device placed upwind. Such differences in chip temperature are considered to be caused by the effects of thermal conduction (including interference) and air (thermal convection).

Data:



Note 1: Relative chip temperature $T_{ch} = \text{each_chip_temperature} / \text{Baseline_chip_temperature} \times 100\text{ }(\%)$

Note 2: Relative to a baseline model placed upwind with an air velocity of 1 m/s and 5 mm spacing

17. Effects of cooling air velocity and device placement (e.g., correlation between physically large and small devices)

Question: How much do air velocity and the placement of physically large and small devices affect the thermal resistance?

Conditions:

Package: SOP Advance (small device)

TO-220SM(W) (large device)

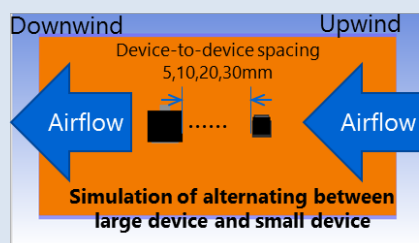
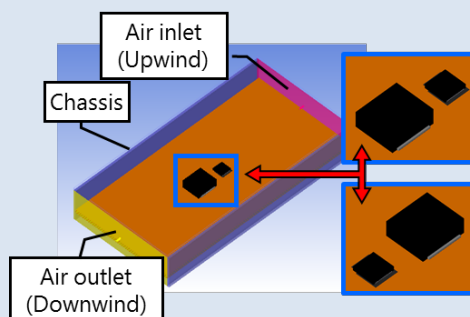
Conditions: $T_a = 25^\circ$, $P_D = 5.0$ W (both large and small devices),

forced air cooling (air velocity: 1, 3, and 5 m/s)

Board: Four-layer board (2 × 1 inches), 1.6 mm thick

Cu coverage: 100% (35 μ m thick) on all layers

Chassis: 101.6×51.8 mm, 15.6 mm high, 1.0 mm thick



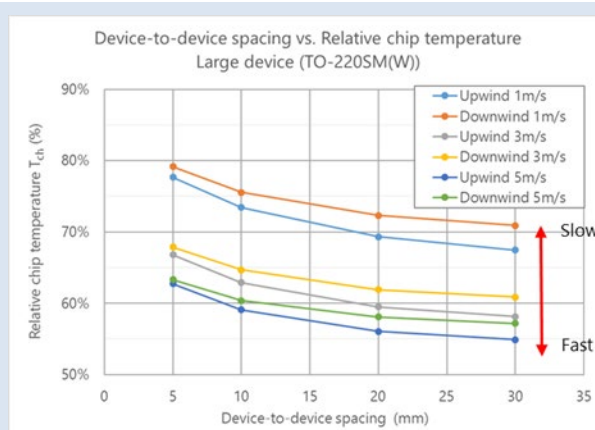
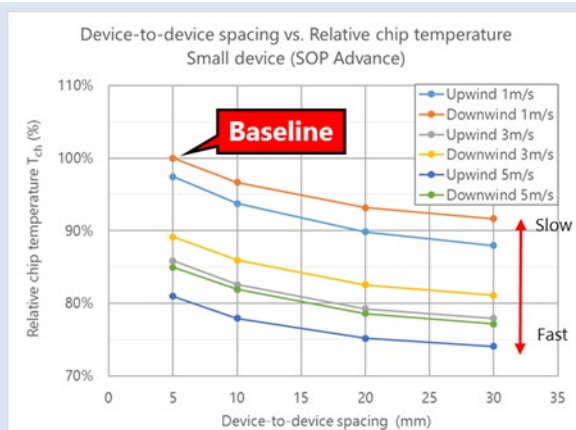
Top view (The top surface is not shown)

Conclusion: Placing a small device upwind provides a greater reduction in chip temperature.

Results: The chip temperatures of physically large and small devices differ because air strikes them in a different manner.

- The higher the air velocity, the higher the cooling effect.
- The chip temperature of the device with a larger surface area becomes lower.
- Chip temperature decreases as device-to-device spacing increases, but levels off at a certain distance.
- Although it is beneficial to place a small device upwind, placing a large device upwind has only a small positive effect. It is necessary to take the device size into consideration when a board has both small and large devices.

Data:



Note 1: Relative chip temperature $T_{ch} = \text{each_chip_temperature} / \text{baseline_chip_temperature} \times 100$ (%)

Note 2: Relative to a model with the small device placed upwind with an air velocity of 1m/s and 5 mm spacing

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