Quick Reference Guide for Thermal Design for Power Semiconductor SMD type

SMD：Surface Mount Device

Outline:

This application note is a supplement to other documents about thermal design. The information contained herein is more concise and easier to understand and shows only thermal tendencies using simplified models.

Table of Contents

0. Introduction: Quick Reference Guide for Thermal Design for Power Semiconductor SMD type

0.1. Background

Power Semiconductor SMD type in automotive and high-power electronic applications are becoming exposed to increasingly high temperature because of 1) a reduction in system size, 2) an increase in board assembly density, and 3) an increase in system power consumption due to performance enhancement. It is therefore important to grasp the thermal profile of your system design in the early stages of development. Under these circumstances, Toshiba provides several application notes on its website to help you reduce chip temperature and thereby facilitate thermal design. Lately, Toshiba released *Hints and Tips for Thermal Design for Discrete Semiconductor Devices — Part 2* that provides the results of simulations using natural convection models and *Hints and Tips for Thermal Design for Discrete Semiconductor Devices — Part 3* that summarizes the results of simulations using forced-convection models that emulate real hardware conditions more closely. Since these application notes were published, we have received feedback from their readers, saying that they need a handy at-a-glance guide to know just enough about thermal design quickly.

The *Quick Reference Guide for Thermal Design for Power Semiconductor SMD type* provides at-a-glance information as a supplement to other application notes. It shows only thermal tendencies using simplified models. The device and board models used herein are identical to the simplified models used in the previous application notes. The board model used as a baseline represents a 1.6-mm-thick four-layer board with a trace thickness of 35 µm. The *Quick Reference Guide for Thermal Design for Discrete Semiconductor Devices* is formatted as questions and answers, using as a reference the results of analyses contained in *Hints and Tips for Thermal Design for Discrete Semiconductor Devices, Part 2* and *Part 3*.

We hope this quick reference guide will be your useful companion for understanding thermal behavior.

0.2. Summary

The following table summarizes the simulation results. You can confirm the tendencies in thermal resistance that were revealed by simulation in the following table.

Contents	Countermeasure	Reduction in thermal resistance
1. Board size vs. thermal resistance	Increasing the board size	Four-layer board one inch square ⇒ four-layer board two inches square: 47% reduction (Effective for boards up to two inches square)
2. Number of board layers vs. thermal resistance	Increasing the number of board layers	4 layers ⇒ 8 layers: 14% reduction
3. Trace thickness on outer board layers vs. thermal resistance	Increasing the thickness of traces on outer layers	35 µm ⇒ 105 µm: 13% reduction
4. Board Cu coverage vs. thermal resistance #1	Increasing Cu coverage	20% ⇒ 100%: 45% reduction
5. Board Cu coverage vs. thermal resistance #2	Increasing the width of board traces near heat sources	Narrow traces ⇒ Wide traces : 4% reduction
6. Number of vias just below E-pad vs. thermal resistance	Increasing the number of thermal vias just below E-pad	0 vias ⇒ 9 vias: 26% reduction
7. Number of vias on the periphery of a device vs. thermal resistance	Increasing the number of vias on the periphery of a device	0 vias ⇒ 10 vias: 15% reduction
8. Spacing between the package mold and vias on its periphery vs. thermal resistance	Placing thermal vias close to the package mold on its periphery	3.0 mm ⇒ 0.6 mm: 16% reduction
9. Vias just below E-pad (inner vias) and vias on the periphery of a device (outer vias) vs. thermal resistance	Vias just below E-pad have a greater effect in reducing thermal resistance.	10 outer vias ⇒ 9 inner vias: 9% reduction
10. Device-to-device spacing vs. thermal resistance	Increasing device-to-device spacing reduces thermal interference.	0.5 mm ⇒ 10 mm: 20% reduction
11. Countermeasures for thermal interference vs. thermal resistance	Adding thermal vias between devices	No vias between devices ⇒ Adding vias: 10% reduction
12. Effects of a heatsink on thermal resistance	A heatsink helps reduce thermal resistance. The combined use of a heatsink and thermal vias provides a greater effect.	No heatsink ⇒ Adding a heatsink: 25% reduction
13. Board orientation vs. thermal resistance	In the case of natural air convection, placing a board in the upright position helps reduce thermal resistance.	Board facing up ⇒ Upright landscape orientation: 9% reduction
14. Temperature distribution on the mold surface #1	(Care should be taken as to the monitor position because the mold surface has a temperature gradient.)	—
15. Temperature distribution on the mold surface #2	(Temperature stabilizes when metal tape is affixed on the mold surface.)	—
16. Air velocity along a model with a heatsink vs. thermal resistance	Thermal resistance decreases greatly when airflow hits a heat sink in the right direction.	No airflow ⇒ 1-m/s air velocity: 34% reduction

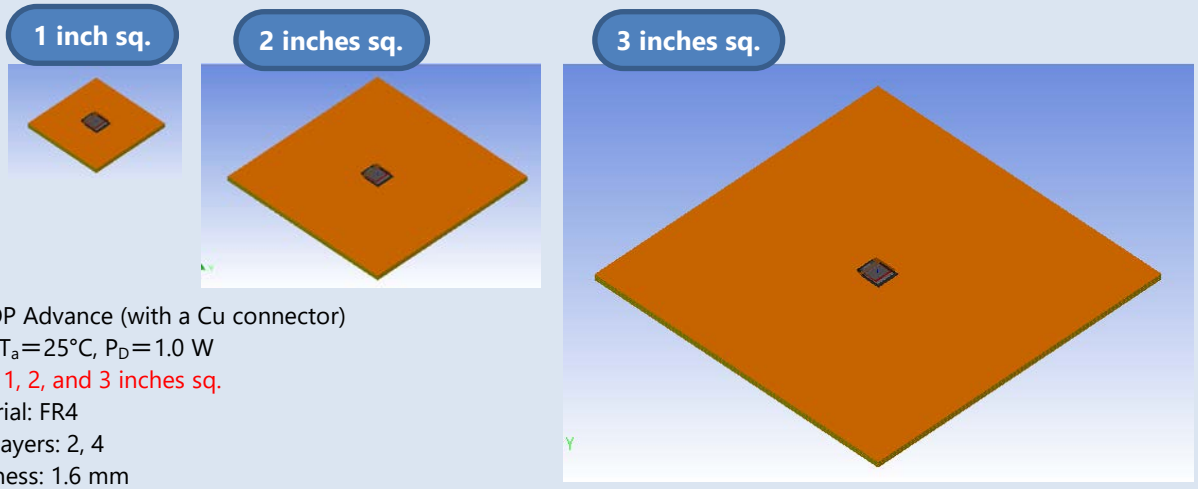
Note 1: Cu coverage means the ratio of the area occupied by board traces to the total board area

Note 2: E-pad stands for “an exposed pad.” It is a metal pad exposed on the bottom of a package.

1. Board size vs. thermal resistance

Question: How much does the board size affect the thermal resistance?

Conditions:

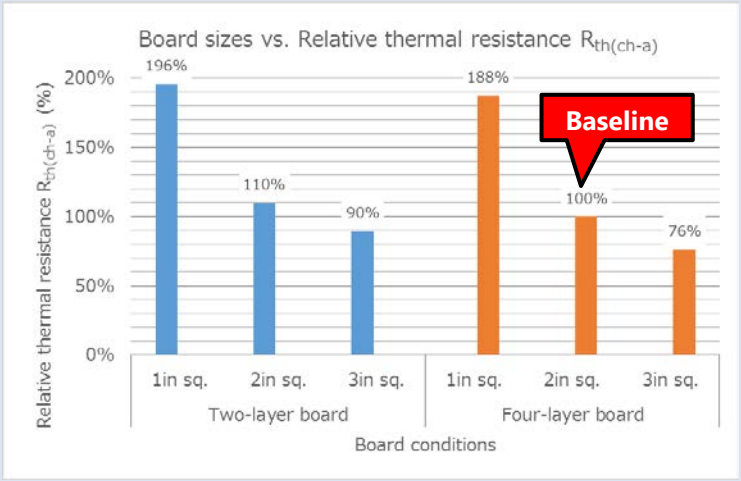


Package: SOP Advance (with a Cu connector)
Conditions: T_a=25°C, P_D=1.0 W
Board sizes: 1, 2, and 3 inches sq.
Board material: FR4
Number of layers: 2, 4
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers

Conclusion: Increasing the board size, particularly up to two inches square, is beneficial in reducing thermal resistance.

Results: Increasing the board size helps reduce the thermal resistance. This is due to the increased heat dissipation from the board. A board two inches square provides a considerably lower thermal resistance than a board one inch square, but a board three inches square does not produce such a significant effect. (A four-layer board two inches square results lower thermal resistance than a four-layer board one inch square.) Boards up to two inches square provide a significant reduction in thermal resistance.

Data:



Structure (Number of layers)	Size (inches sq.)	Relative thermal resistance
2	1	196%
	2	110%
	3	90%
4	1	188%
	2	100%
	3	76%

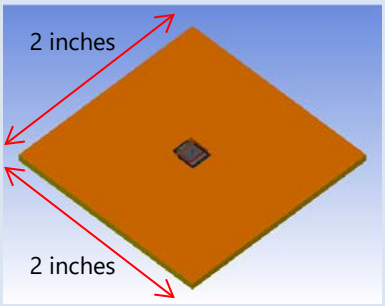
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) =(each_thermal_resistance / baseline_thermal_resistance)× 100 (%)
Note 2: Relative to a baseline model of a four-layer board two inches square

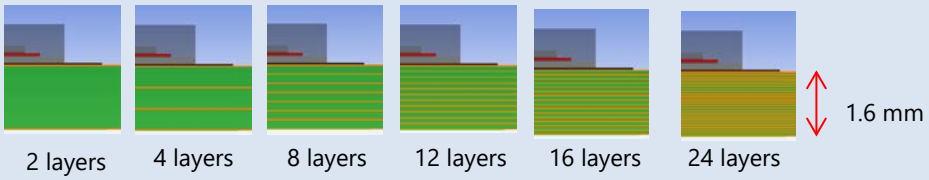
2. Number of board layers vs. thermal resistance

Question: How much does the number of board layers affect the thermal resistance?

Conditions:

Package: SOP Advance
(with a Cu connector)
Conditions: $T_a = 25°C$, $P_D = 1.0$ W
Number of layers: 2 to 24 (See the figures below.)
Board material: FR4
Board size: 2 inches sq.
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers



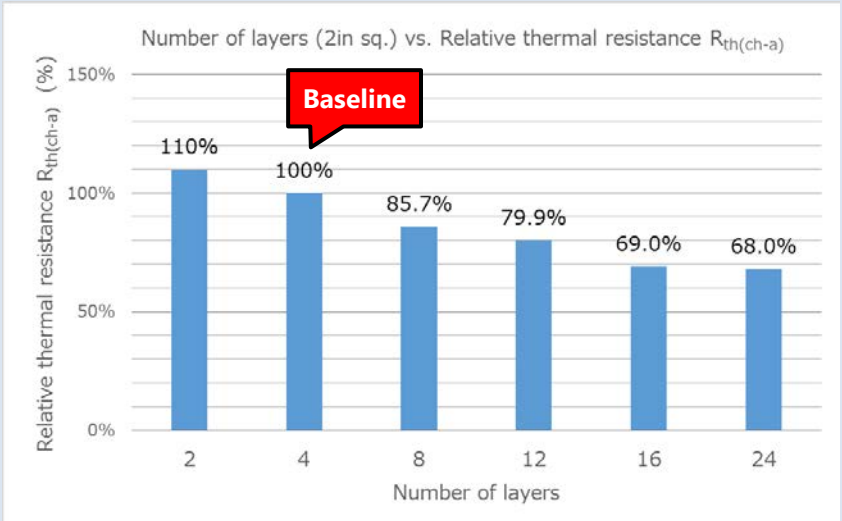


2 layers 4 layers 8 layers 12 layers 16 layers 24 layers

Conclusion: Increasing the number of board layers helps reduce the thermal resistance.

Results: When the board size is equal, increasing the number of board layers helps reduce the thermal resistance. (An eight-layer board results in 14.3% lower thermal resistance than a four-layer board.) This is due to an increase in the heat dissipation to a board because of the increased copper traces. The reductions in thermal resistance level off when the number of layers exceeds 16.

Data:



Number of layers	Relative thermal resistance
2	110%
4	100%
8	85.7%
12	79.9%
16	69.0%
24	68.0%

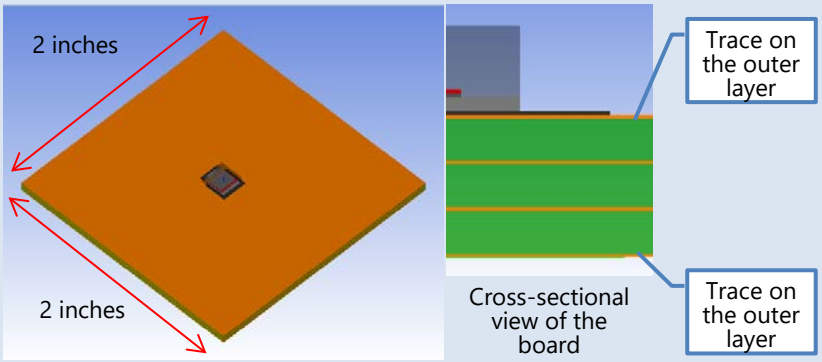
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to a baseline model of a four-layer board two inches square

3. Trace thickness on outer board layers vs. thermal resistance

Question: How much does the trace thickness on the outer layers of a board affect the thermal resistance?

Conditions:

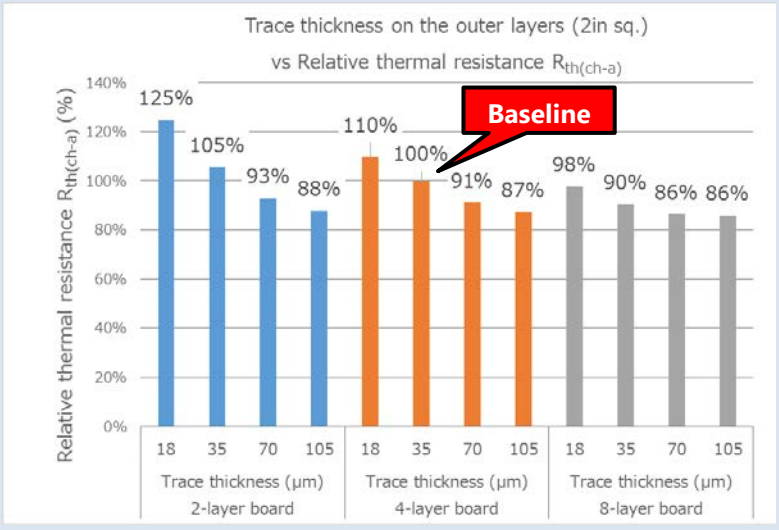
Package: SOP Advance
(with a Cu connector)
Conditions: T_a = 25°C, P_D = 1.0 W
Board size: 2 inches sq.
Number of layers: 2, 4, 8
Board thickness: 1.6 mm
Package: SOP Advance
Cu coverage: 100% on all layers
Trace thickness on the outer layers:
18 to 105 µm
Trace thickness on the inner layers:
35 µm



Conclusion: Increasing the trace thickness on the outer layers of a board helps reduce the thermal resistance. This effect diminishes as the number of board layers increases.

Results: Increasing the trace thickness on the outer layers (i.e., top and bottom layers) of a board helps reduce the thermal resistance. (A board with a trace thickness of 105 µm results in 13% lower thermal resistance than a board with a trace thickness of 35 µm.) However, boards with a greater number of inner layers provide less reduction in thermal resistance. In the case of a two-layer board, maximizing the trace thickness is beneficial.

Data:



Trace thickness on the outer layers	Relative thermal resistance ($R_{th(ch-a)}$)		
	2-layer board	4-layer board	8-layer board
18 µm	125%	110%	98%
35 µm	105%	100%	90%
70 µm	93%	91%	86%
105 µm	88%	87%	86%

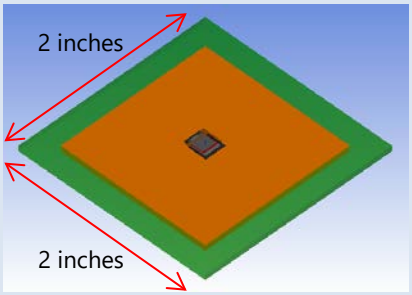
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to a baseline model of a board two inches square with a trace thickness of 35 µm

4. Board Cu coverage vs. thermal resistance #1

Question: How much does the Cu coverage of a board affect the thermal resistance?

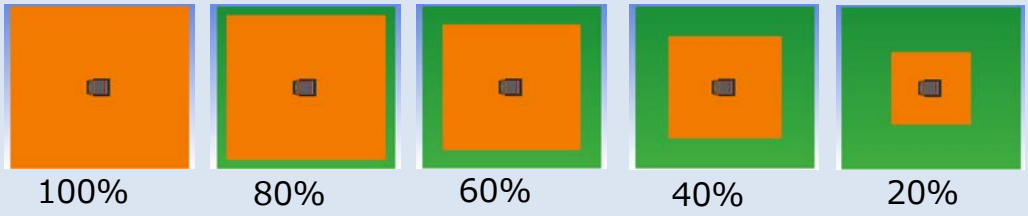
Conditions:

Package: SOP Advance (with a Cu connector)
Conditions: $T_a = 25°C$, $P_D = 1.0$ W
Cu coverage: 20 to 100% on all layers (See the figures below.)
Number of layers: 2, 4, 8
Board size: 2 inches sq.
Board thickness: 1.6 mm
Trace thickness: 35 µm on all layers



Example: Model with 60% Cu coverage

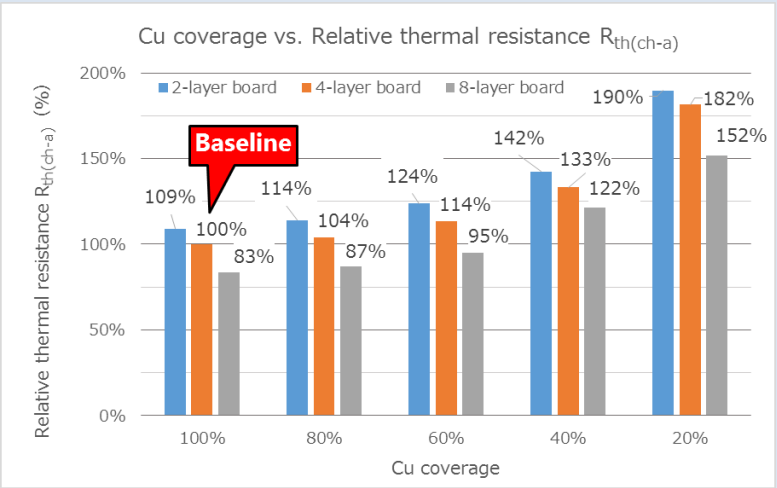
Boards with different Cu coverage



Conclusion: Boards with more Cu coverage result in lower thermal resistance.

Results: Boards with more Cu coverage result in lower thermal resistance. (A board with 100% Cu coverage results lower thermal resistance than a board with 20% Cu coverage.) This tendency is not affected by the number of board layers. This is because boards with more Cu coverage have more area to which heat from a device can dissipate.

Data:



Coverage	Relative thermal resistance		
	2-layer board	4-layer board	8-layer board
100%	109%	100%	83%
80%	114%	104%	87%
60%	124%	114%	95%
40%	142%	133%	122%
20%	190%	182%	152%

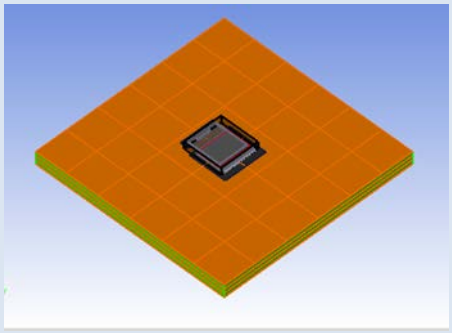
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to a baseline model with 100% Cu coverage

5. Board Cu coverage vs. thermal resistance #2

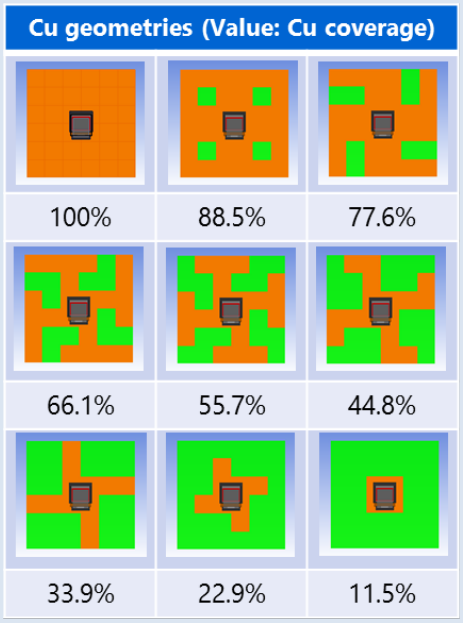
Question: How much do Cu geometries on a board affect the thermal resistance?

Conditions:

Package: SOP Advance (with a Cu connector)
Conditions: T_a = 25°C, P_D = 0.5 W
Cu coverage: 11.5 to 100% on all layers
(See the right-hand figures.)
Number of layers: 4
Board thickness: 1.6 mm
Trace thickness on the outer layers: 70 µm
Trace thickness on the inner layers: 35 µm



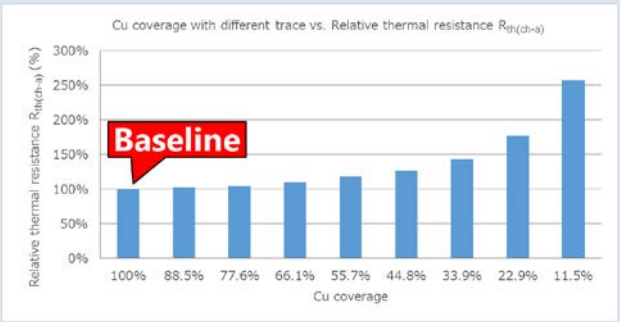
Models with different Cu



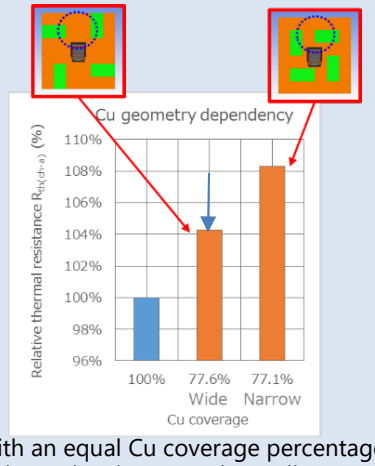
Conclusion: Boards with higher Cu coverage result in lower thermal resistance, irrespective of Cu geometries. Increasing the width of traces near a heat source helps reduce thermal resistance.

Results: As is the case with square Cu coverage, boards with less Cu coverage result in higher thermal resistance regardless of Cu geometries. Even two boards with an equal Cu coverage percentage could result in different thermal resistances, depending on Cu geometries. (The board with wide Cu coverage resulted in 4% lower thermal resistance than the board with narrow Cu coverage.) Cu traces in the vicinity of a heat source are important.

Data:



Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to a baseline model with 100% Cu coverage



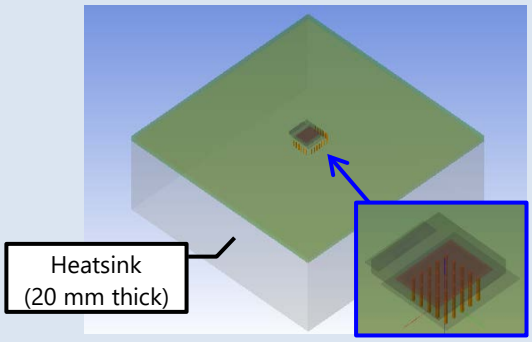
Boards with an equal Cu coverage percentage result in different thermal resistances, depending on Cu geometries. The area highlighted by a circle has a significant effect.

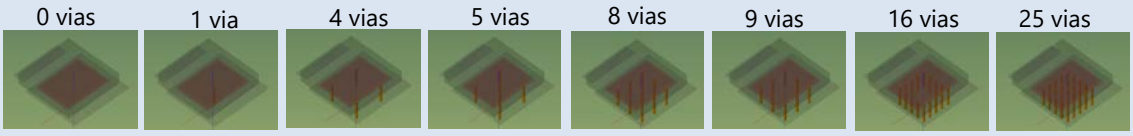
6. Number of vias just below E-pad vs. thermal resistance

Question: How much do the number and size of vias just below a device affect its thermal resistance?

Conditions :

Package: SOP Advance
(with a Cu connector)
Conditions: T_a = 25°C, P_D = 1.0 W
Number of vias: 0 to 25 (See the figures below.)
Number of layers: 4
Board size: 2 inches sq.
Board thickness:1.6 mm
Cu coverage: 100% (35 µm thick) on all layers

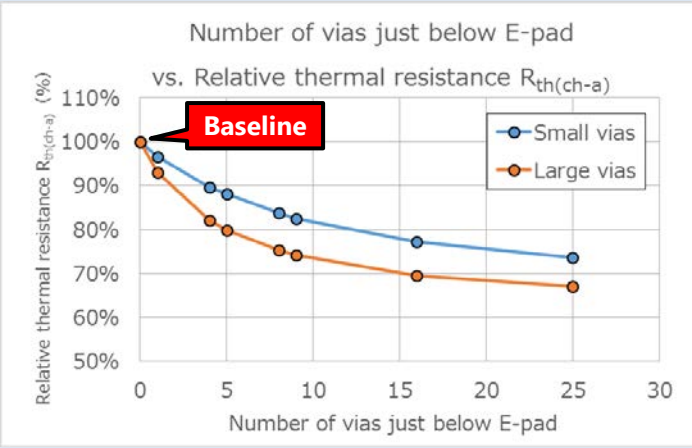




Conclusion: Increasing the number and size of thermal vias just below E-pad helps reduce the thermal resistance.

Results: Increasing the number of thermal vias just below E-pad helps increase heat dissipation from the backside of a board, reducing the thermal resistance. (A board with nine large vias results in 26% lower thermal resistance than a board with zero vias.) In addition, larger vias are more effective in reducing thermal resistance.

Data:



Number of vias just below E-pad	Relative thermal resistance ($R_{th(ch-a)}$)	
	Small vias	Large vias
0	100%	100%
1	97%	93%
4	90%	82%
5	88%	80%
8	84%	75%
9	82%	74%
16	77%	69%
25	74%	67%

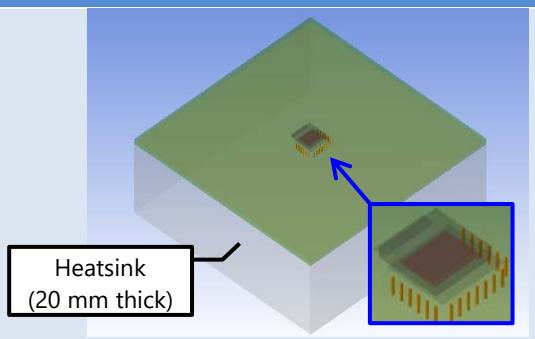
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Small vias: φ300 µm, 25-µm-thick inner plating
Note 3: Large vias: φ450 µm, 50-µm-thick inner plating
Note 4: Relative to a baseline model with zero vias

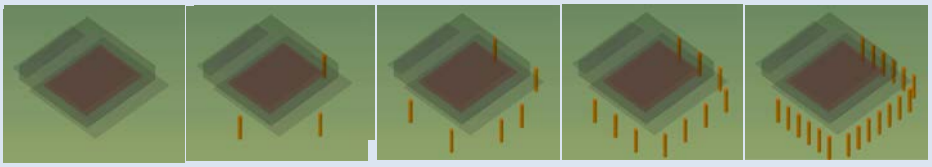
7. Number of vias on the periphery of a device vs. thermal resistance

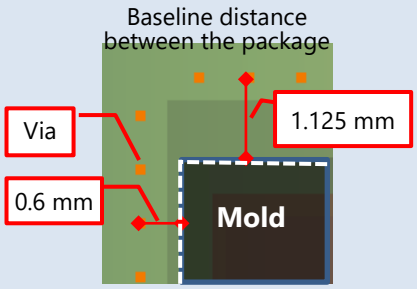
Question: How much do the number and size of vias on the periphery of a device affect its thermal resistance?

Conditions:

Package: SOP Advance (with a Cu connector)
Conditions: $T_a = 25°C$, $P_D = 1.0$ W
Number of vias: 0 to 19 (See the figures below.)
Number of layers: 4
Board size: 2 inches sq.
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers



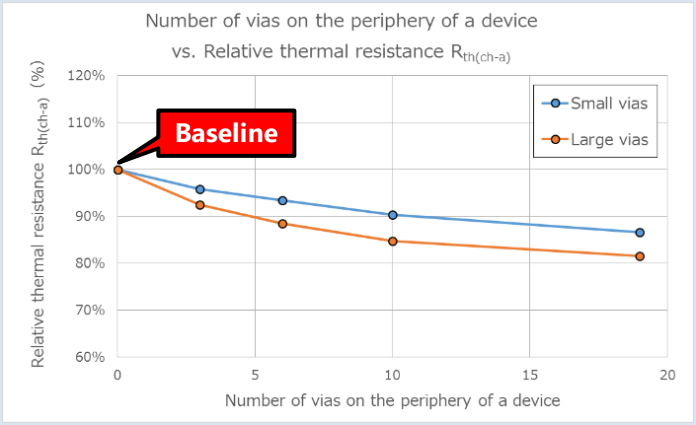




Conclusion: Increasing the number and size of thermal vias on the periphery of a device helps reduce its thermal resistance.

Results: Increasing the number of vias on the periphery of a device helps reduce its thermal resistance. (A board with 10 large vias results in 15% lower thermal resistance than a board with zero vias.) As is the case with vias just below E-pad, larger vias are more effective in reducing thermal resistance.

Data:



Number of vias on the periphery of a device	Relative thermal resistance ($R_{th(ch-a)}$)	
	Small vias	Large vias
0	100%	100%
3	96%	92%
6	93%	88%
10	90%	85%
19	87%	82%

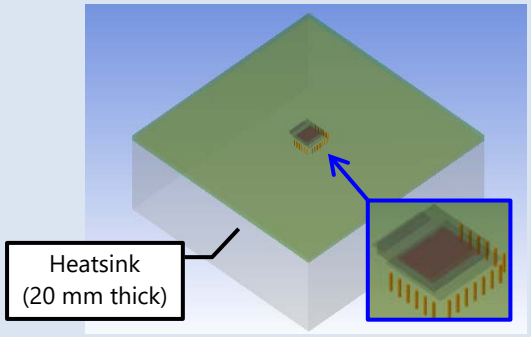
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Small vias: φ300 µm, 25-µm-thick inner plating
Note 3: Large vias: φ450 µm, 50-µm-thick inner plating
Note 4: Relative to a baseline model with zero vias

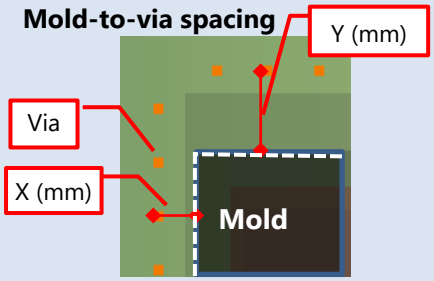
8. Spacing between the package mold and vias on the periphery of a device vs. thermal resistance

Question: How much do vias on the periphery of a device affect its thermal resistance?

Conditions:

Package: SOP Advance (with a Cu connector)
Conditions: $T_a = 25°C$, $P_D = 1.0$ W
Mold-to-via spacing: See the figure below.
Number of outer vias: 19
Number of layers: 4
Board size: 2 inches sq.
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers





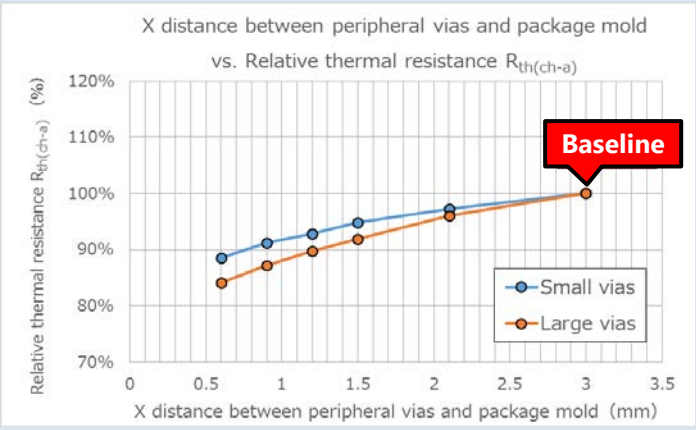
(mm)

X distance, Y distance						
X distance	0.600	0.900	1.200	1.500	2.100	3.000
Y distance	1.125	1.425	1.725	2.025	2.625	3.525

Conclusion: Placing thermal vias close to a device helps reduce its thermal resistance.

Results: Large vias in the vicinity of a device help reduce its thermal resistance. (Large vias placed at a distance of 0.6 mm from a device result in 16% lower resistance than those placed at a distance of 3.0 mm.)

Data:



X distance between peripheral vias and package mold (mm)	Relative thermal resistance ($R_{th(ch-a)}$)	
	Small vias	Large vias
0.6	89%	84%
0.9	91%	87%
1.2	93%	90%
1.5	95%	92%
2.1	97%	96%
3.0	100%	100%

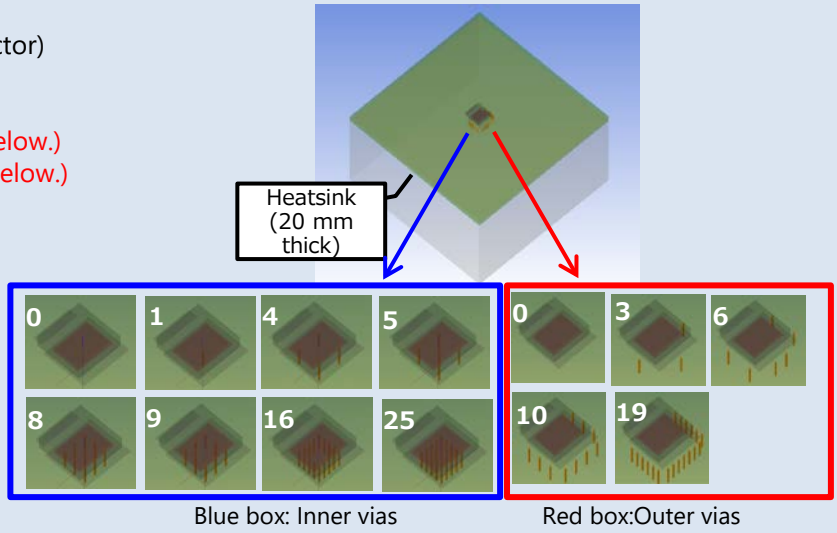
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Small vias: φ300 µm, 25-µm-thick inner plating
Note 3: Large vias: φ450 µm, 50-µm-thick inner plating
Note 4: Relative to a baseline model with an X distance of 3.0 mm

9. Vias just below E-pad (inner vias) and vias on the periphery of a device (outer vias) vs. thermal resistance

Question: How do vias just below a device and those on its periphery affect its thermal resistance?

Conditions:

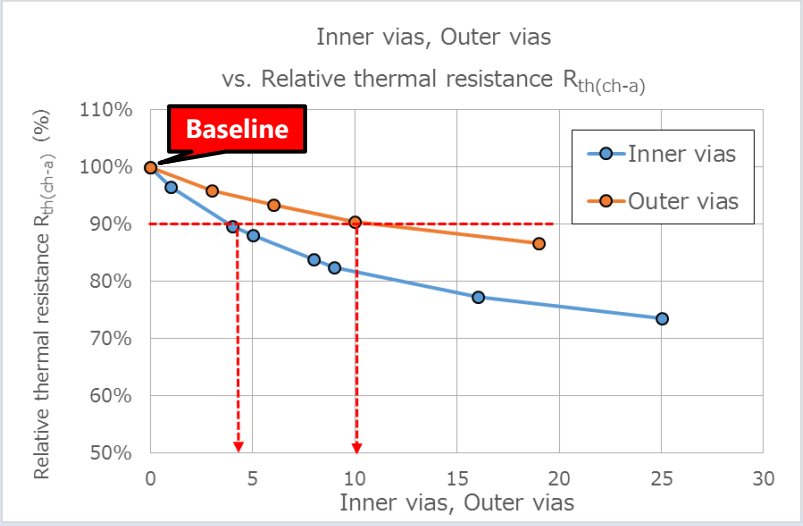
Package: SOP Advance (with a Cu connector)
Conditions: T_a = 25°C, P_D = 1.0 W
Number of vias:
Inner vias: 0 to 25 (See the figures below.)
Outer vias: 0 to 19 (See the figures below.)
Number of layers: 4
Board size: 2 inches sq.
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers



Conclusion: Placing vias just below E-pad is more effective in reducing the thermal resistance.

Results: Placing vias just below E-pad is more effective in reducing the thermal resistance of a device. (Thermal resistance is reduced from 90% to 82% when the vias condition changes from ten outer vias to nine inner vias.) An equal reduction in thermal resistance can be achieved with less than half the number of inner vias.

Data:



Number of vias		Relative thermal resistance ($R_{th(ch-a)}$)
None	0	100%
Inner vias	1	97%
	4	90%
	5	88%
	8	84%
	9	82%
	16	77%
	25	74%
Outer vias	3	96%
	6	93%
	10	90%
	19	87%

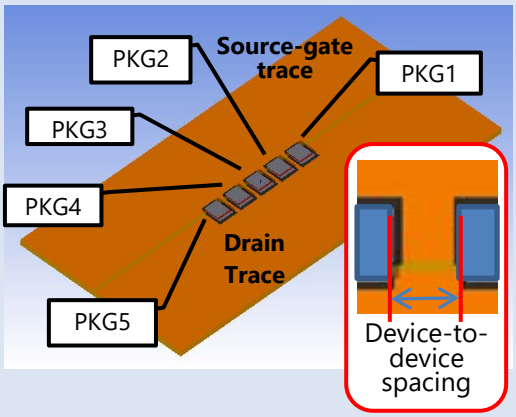
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Small vias: φ300 µm, 25-µm-thick inner plating
Note 3: Relative to a baseline model with zero vias

10. Device-to-device spacing vs. thermal resistance

Question: How does device-to-device spacing affect thermal resistance?

Conditions:

Number of devices: 5
Package: SOP Advance (with a Cu connector)
Conditions: T_a = 25°C, P_D = 1.0 W per device
Spacing: 0.5 to 10 mm (See the figures below.)
Number of layers: 4
Board size: 4 × 2 inches
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers

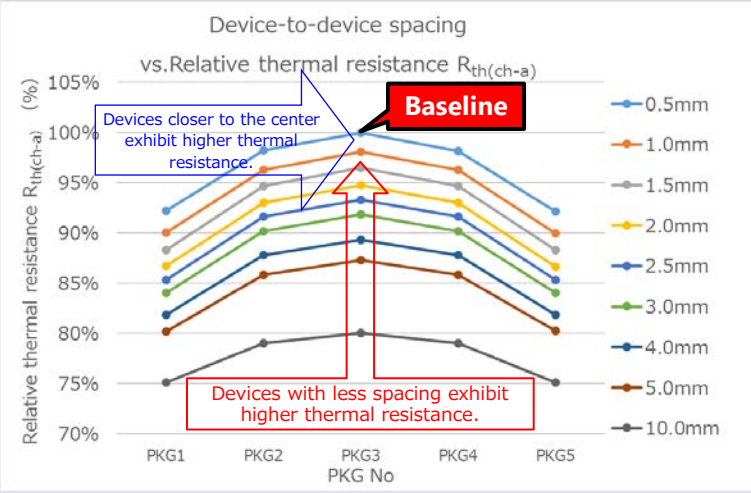


Device-to-device spacing:

Conclusion: Reducing device-to-device spacing increases thermal resistance because of the effect of thermal interference.

Results: When multiple devices arranged in a row dissipate the same amount of power, reducing the device-to-device spacing results in an increase in thermal resistance. (The devices exhibit 20% lower thermal resistance when placed with 10-mm spacing than when placed with 0.5-mm spacing.) A device placed between two other devices exhibits a greater increase in thermal resistance. This is because such a device is affected by thermal interference due to the heat from both sides.

Data:



Spacing (mm)	Relative thermal resistance ($R_{th(ch-a)}$)				
	PKG1	PKG2	PKG3	PKG4	PKG5
0.5	92%	98%	100%	98%	92%
1.0	90%	96%	98%	96%	90%
1.5	88%	95%	96%	95%	88%
2.0	87%	93%	95%	93%	87%
2.5	85%	92%	93%	92%	85%
3.0	84%	90%	92%	90%	84%
4.0	82%	88%	89%	88%	82%
5.0	80%	86%	87%	86%	80%
10.0	75%	79%	80%	79%	75%

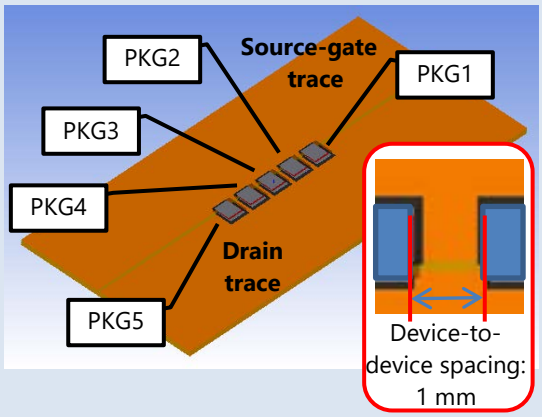
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to a baseline model at the center (PKG3) with 0.5-mm device-to-device spacing

11. Countermeasures for thermal interference vs. thermal resistance

Question: How to reduce thermal interference between devices?

Conditions:

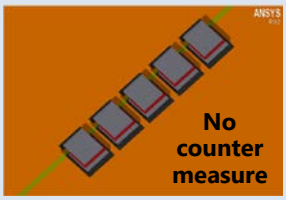
Number of devices: 5
Package: SOP Advance (with a Cu connector)
Conditions: T_a = 25°C, P_D = 1.0 W per device
Number of layers: 4
Board size: 4 × 2 inches
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers
Device-to-device spacing: 1 mm
Traces between devices are cut.
Vias between devices are modeled with solid traces.

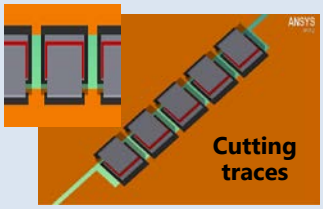


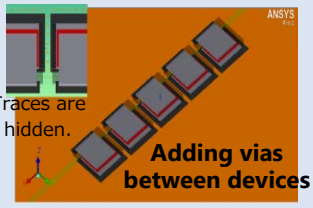
Conclusion: Adding vias between devices helps reduce their thermal interference.

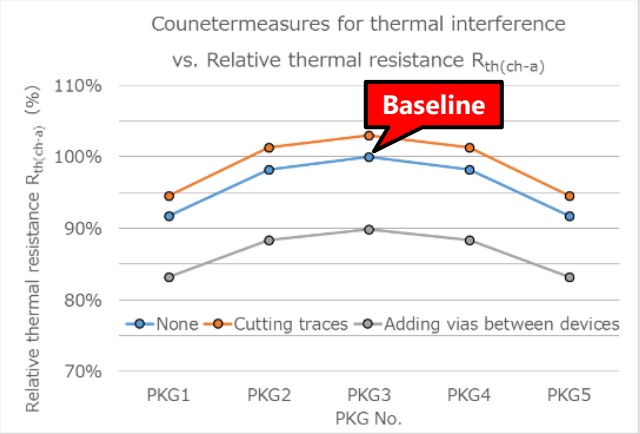
Results: The above results compare the effects of two countermeasures for thermal interference. Cutting traces between devices results in a reduction in heat dissipation from the devices. This does not help reduce their thermal interference and leads to an increase in thermal resistance. Care should be exercised in cutting traces between heat-generating devices. In contrast, vias on the periphery of devices help reduce the amount of heat flowing from adjacent devices. These vias help reduce thermal interference between devices and increase heat dissipation to other layer traces. (No vias between devices ⇒ Adding vias: 10% reduction)

Data: Examples of countermeasures for thermal interference









Countermeasure for thermal interference	Relative thermal resistance ($R_{th(ch-a)}$)				
	PKG1	PKG2	PKG3	PKG4	PKG5
None	92%	98%	100%	98%	92%
Cutting traces	95%	101%	103%	101%	95%
Adding vias between devices	83%	88%	90%	88%	83%

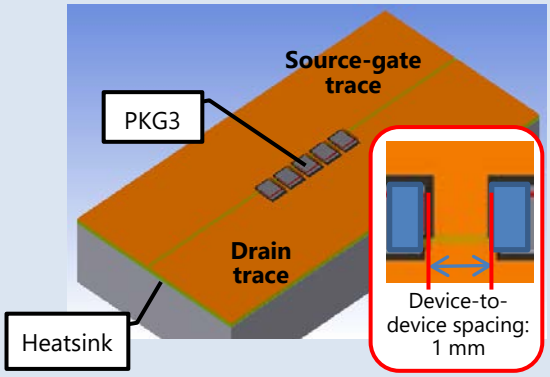
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) =(each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to the device model at the center (PKG3) without any countermeasure

12. Effects of a heatsink on thermal resistance

Question: How effective is a heatsink? What is an effective way of using a heatsink?

Conditions:

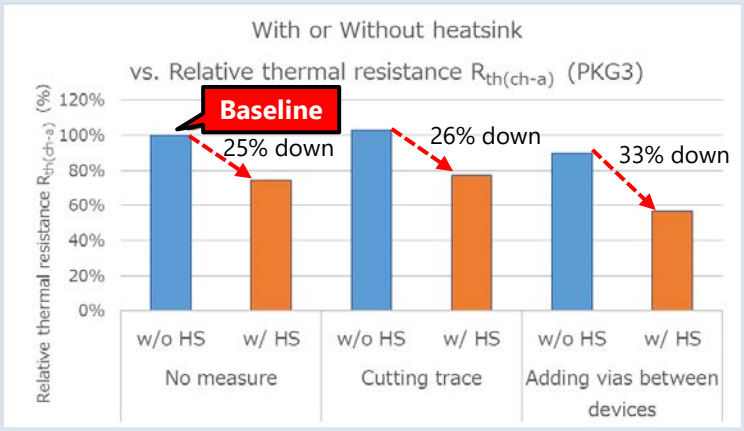
Package: SOP Advance (with a Cu connector)
Conditions: T_a = 25°C,
P_D = 1.0 W per device
Number of layers: 4
Board size: 4 × 2 inches
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers
Device-to-device spacing: 1mm
Heatsink: 4 × 2 inches, d = 20 mm
Traces between devices are cut.
Vias between devices are modeled with solid traces.

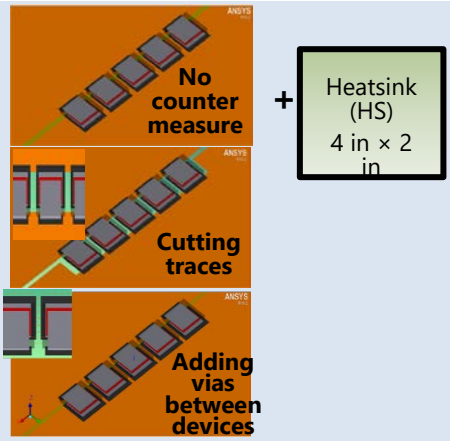


Conclusion: A heatsink considerably reduces the thermal resistance. Combining a heatsink with vias helps further reduce thermal interference and therefore thermal resistance.

Results: Thermal resistance can be further reduced by attaching a heatsink on the backside of a board in addition to implementing a countermeasure for thermal interference. A heatsink has a significant effect on the vias that conduct heat to the backside of the board. (No heatsink ⇒ Adding a heatsink: 25% reduction; No heatsink ⇒ Adding a heatsink and vias between devices: 43% reduction)

Data: **Effects of a heatsink**





Countermeasure	PKG1		PKG2		PKG3		PKG4		PKG5	
	w/o HS	w/ HS	w/o HS	w/ HS	w/o HS	w/ HS	w/o HS	w/ HS	w/o HS	w/ HS
No measure	92%	68%	98%	73%	100%	75%	98%	73%	92%	68%
Cutting traces	95%	70%	101%	76%	103%	77%	101%	76%	95%	70%
Adding vias between devices	83%	54%	88%	56%	90%	57%	88%	56%	83%	54%

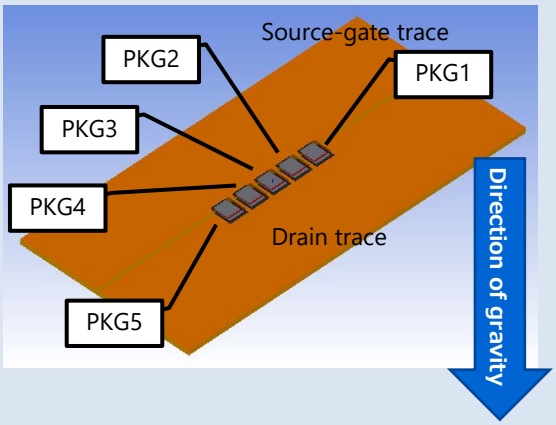
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to the device model at the center (PKG3) without a heatsink and a countermeasure for thermal interference

13. Board orientation vs. thermal resistance

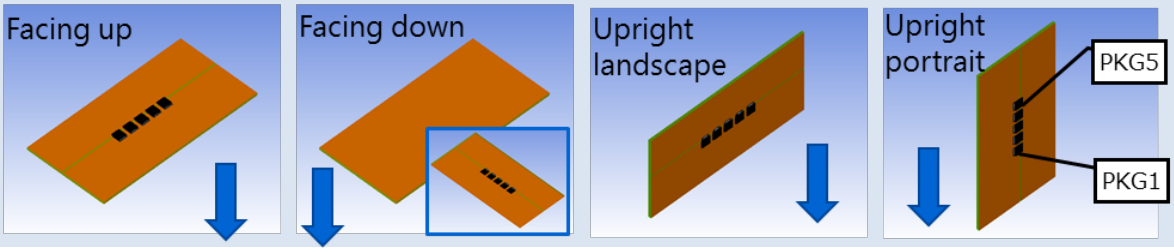
Question: How much does the board orientation affect thermal resistance?

Conditions:

Number of devices: 5
Package: SOP Advance (with a Cu connector)
Conditions: T_a = 25°C, P_D = 1.0 W per device
Number of layers: 4
Board size: 4 × 2 inches
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers
Device-to-device spacing: 1mm
Board orientations: See the figure below.



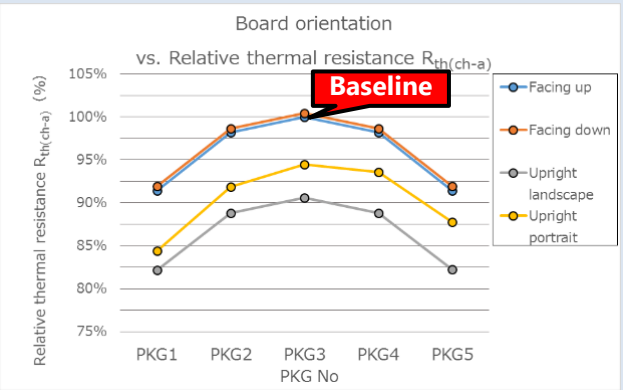
Board orientations



Conclusion: In natural air convection, placing a board in the upright position helps reduce thermal resistance. The landscape orientation is particularly effective.

Results: In natural air convection, devices mounted on the backside of a board (i.e., a board with devices facing down) exhibit the highest thermal resistance. When a board is placed upright in the landscape orientation, the devices exhibit the lowest thermal resistance. (Board placed facing up ⇒ Board placed upright in the landscape orientation: 9.4% reduction) The device model at the center (PKG3) has the highest thermal resistance because of the effects of thermal interference.

Data:



Board Orientation	Relative thermal resistance $R_{th(ch-a)}$ (%)				
	PKG1	PKG2	PKG3	PKG4	PKG5
Facing up	91.4%	98.2%	100%	98.2%	91.4%
Facing down	91.9%	98.6%	100.5%	98.6%	91.9%
Upright landscape	82.2%	88.8%	90.6%	88.8%	82.2%
Upright portrait	84.4%	91.9%	94.5%	93.6%	87.8%

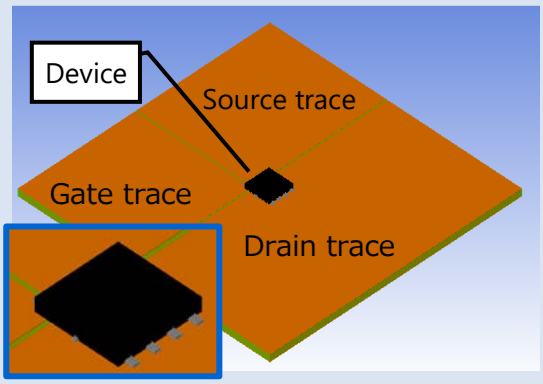
Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to the device model at the center (PKG3) on a board placed with its top side facing up

14. Temperature distribution on the mold surface #1

Question: Where is the mold surface temperature measured?

Conditions:

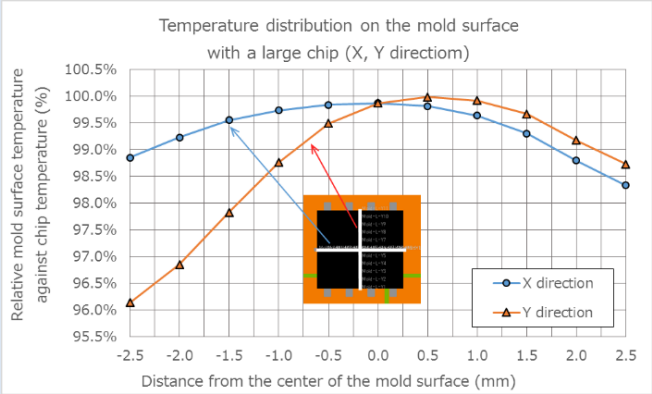
Package: SOP Advance
(with a Cu connector)
Device with a large chip
Device with a small chip
Conditions: $T_a = 25°C$, $P_D = 1.0$ W
Number of layers: 4 (2 inches sq.)
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers

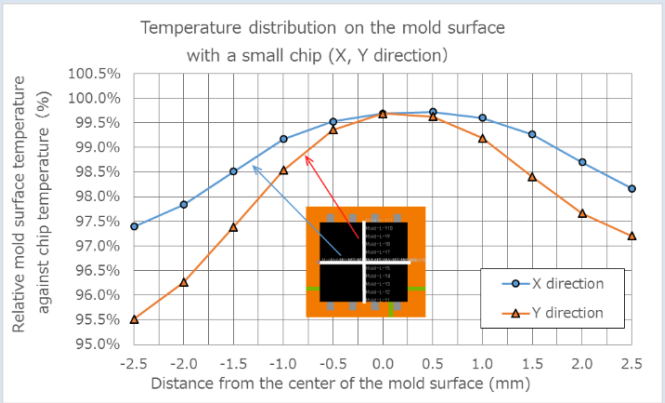


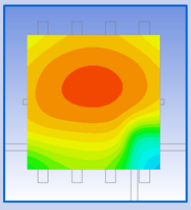
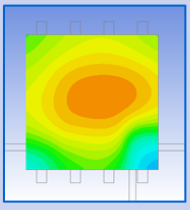
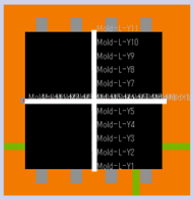
Conclusion: Care should be taken as to the monitor position because the mold surface has a temperature gradient.

Results: There is a difference in temperature at the center and edge of the mold. The temperature distribution images indicate that the center of the mold does not always have the highest temperature. When you use a thermocouple or other temperature probe, you need to exercise care as to which part of the mold becomes hot.

Data:





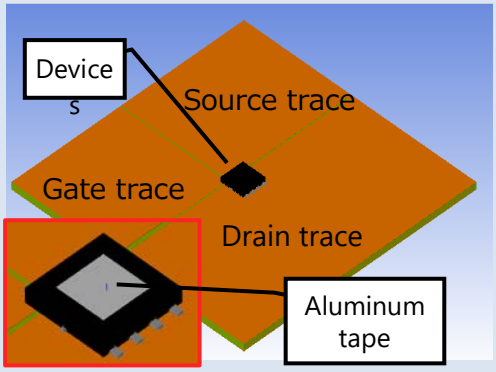
Structure	Large chip located on the center of E-pad	Small chip located on the side of E-pad	Temperature monitor point
Temperature distribution on the mold surface			
Temperature difference on the mold surface	2.03℃	2.24℃	–

15. Temperature distribution on the mold surface #2

Question: How does metal tape affect the temperature distribution on the mold surface?

Conditions:

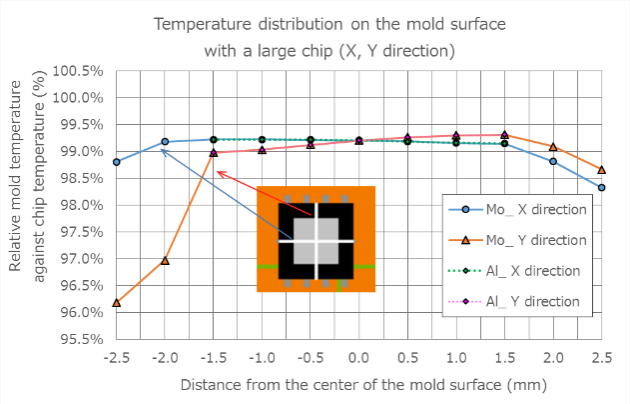
Package: SOP Advance (with a Cu connector)
Device with a large chip
Device with a small chip
Conditions: $T_a = 25°C$, $P_D = 1.0$ W
Number of layers: 4 (2 inches sq.)
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers
Metal tape: Aluminum (50 µm)

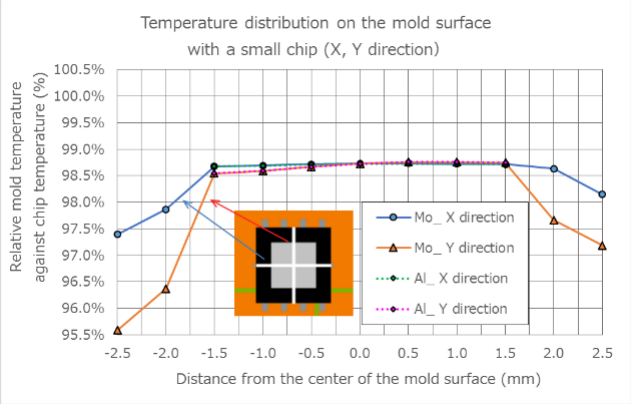


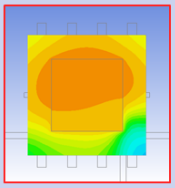
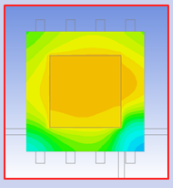
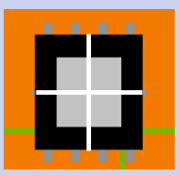
Conclusion: Affixing metal tape on the mold surface makes it possible to take stable temperature measurements.

Results: Affixing metal tape on the top surface of the package mold evens out the temperature distribution under the tape. Note that the metal tape causes the measured temperature to be slightly lower than the chip temperature. The model with a small chip exhibits a temperature that is 1 to 1.5% lower than the chip temperature. However, the benefit of obtaining stable measurements is significant. (In the case of a model with a large chip, the tape surface has a temperature gradient as small as 0.18°C.)

Data:





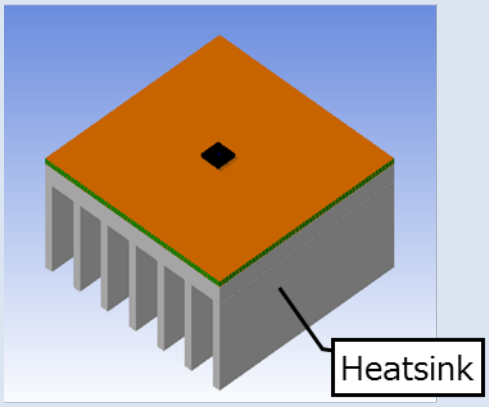
Structure	Large chip located on the center of E-pad	Small chip located on the side of E-pad	Temperature monitor point
Temperature distribution on the mold and Al tape surface			
Temperature difference on the Al tape surface	0.18℃	0.11℃	–

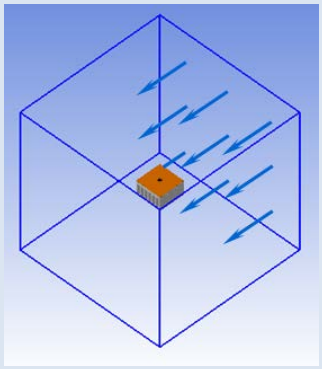
16. Air velocity along a model with a heatsink vs. thermal resistance

Question: How is airflow effective when a heatsink with fins is used?

Conditions:

Package: SOP Advance
(with a Cu connector)
Conditions: T_a = 25°C, P_D = 2.0 W
Number of layers: 4 (2 inches sq.)
Board thickness: 1.6 mm
Cu coverage: 100% (35 µm thick) on all layers
Air velocity: 0 to 10 m/s (See the table below.)



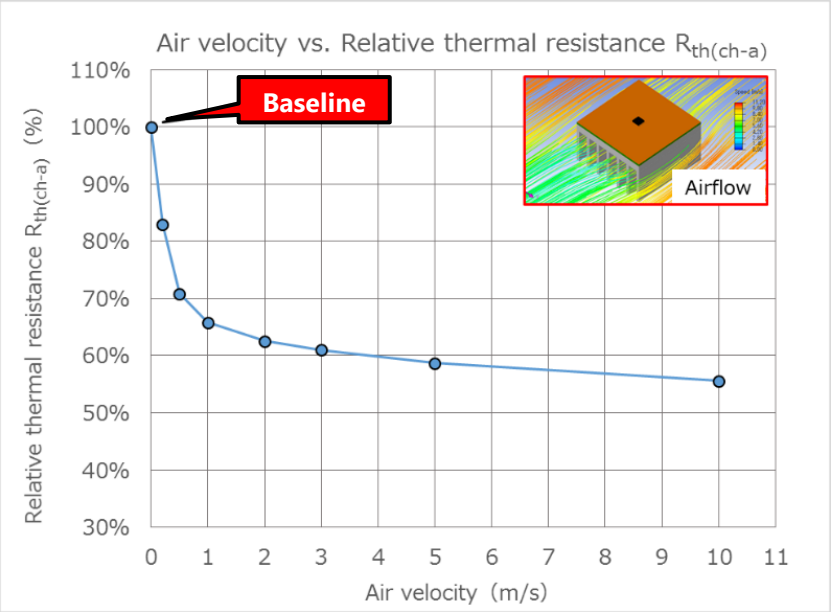


The arrows indicate the direction of airflow.

Conclusion: Thermal resistance decreases greatly when airflow hits a heatsink in the right direction.

Results: Creating airflow in parallel with the fins of the heatsink causes thermal resistance to decrease until the air velocity reaches roughly 1 m/s. (No air flow ⇒ 1-m/s air velocity: 34.2% reduction) When the air velocity exceeds 1 m/s, the thermal resistance curve levels off. When a heatsink with fins is used, airflow helps reduce the thermal resistance considerably.

Data:



Air velocity (m/s)	Relative thermal resistance $R_{th(ch-a)}$
0.0	100%
0.2	83.0%
0.5	70.9%
1.0	65.8%
2.0	62.5%
3.0	61.0%
5.0	58.7%
10	55.6%

Note 1: Relative thermal resistance ($R_{th(ch-a)}$) = (each_thermal_resistance / baseline_thermal_resistance) × 100 (%)
Note 2: Relative to a model with an air velocity of 0 m/s

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE"). ** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

Toshiba Electronic Devices & Storage Corporation
https://toshiba.semicon-storage.com/