

RC Snubbers for Step-Down Converters

Description

This document describes the design and effect of RC snubbers for step-down DC-DC converters.

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1. Snubbers for reducing voltage spikes and ringing in step-down DC-DC converters

Shutting off current in a switching circuit causes a sharp increase in voltage due to stray inductance and self-inductance. In order to reduce a rise in voltage, it is most important to reduce wire stray inductance. This application note describes an alternative way of reducing voltage spikes and ringing using a snubber.

Specifically, this application note focuses on an RC snubber that can be used to suppress voltage spikes and high-frequency ringing produced by the switching of a step-down DC-DC converter (hereinafter simply referred to as a “step-down converter”).

1.1. Operation of a step-down converter and mechanism of voltage spike and ringing generation

Figure 1.1 shows a basic step-down converter circuit, which operates as described below.

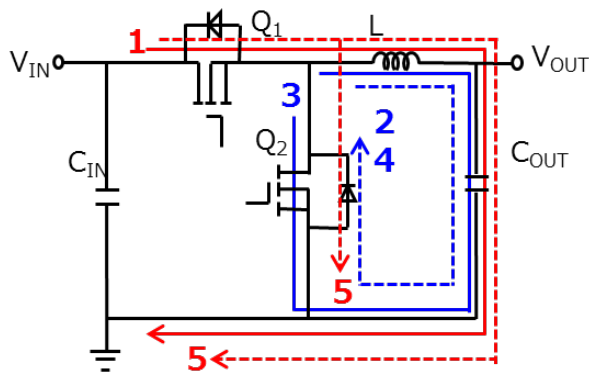


Figure 1.1 Step-down switching converter

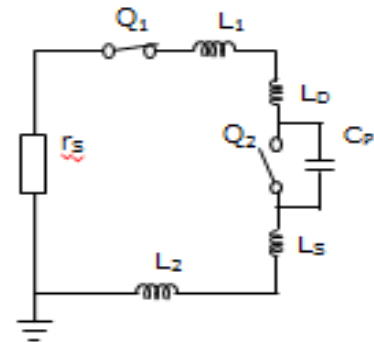


Figure 1.2 Equivalent circuit for the step-down switching converter immediately after the turn-on of Q_1

(1) Basic operation of the step-down converter

The following step numbers correspond to the current path numbers in Figure 1.1.

Step 1. Q_1 turns on and charges the output capacitor C_{OUT} via the inductance L .

Step 2. When Q_1 turns off, a freewheeling current flows through the L - C_{OUT} - Q_2 loop via the body diode of Q_2 .

(This period is a dead time during which both Q_1 and Q_2 are off.)

Step 3. Q_2 turns on, and a current flows through L , C_{OUT} , and Q_2 (from source to drain). (Q_2 operates as a synchronous rectifier.)

Step 4. Q_2 turns off, causing the freewheeling current to flow through its body diode. (This period is a dead time.)

Step 5. Q_1 turns on, causing a current to flow to the inductance L . A reverse recovery current flows through the body diode of Q_2 .

After the current flowing through the body diode of Q_2 disappears, the step-down converter cycles through Steps 1 to 5 again. The output voltage (V_{OUT}) of the step-down converter is determined by

its input voltage (V_{IN}) and the on-duty cycle of Q_1 .

($V_{OUT} \doteq \text{Duty}_{(Q1)} \times V_{IN}$, where $\text{Duty}_{(Q1)}$ is the on-duty cycle of Q_1 .)

(2) Voltage spikes and ringing

At Step 5, the parasitic inductance and capacitance form a resonant circuit, causing transient voltage spikes and ringing. While Q_1 is transitioning to the on state and Q_2 to the off state at Step 5, C_{IN} exhibits a very large capacitance, causing them to be short-circuited. L is also very large and can be considered to be open-circuited. At this time, the step-down converter of Figure 1.1 can be modeled as an equivalent circuit as shown in Figure 1.2.

The main source of the parasitic capacitance (C_P) is the C_{OSS} of Q_2 whereas the sources of the parasitic inductances (L_1 , L_2 , L_D , and L_S) are wires and Q_1 and Q_2 . Let the sum of these inductances be L_P . Then, C_P , L_P , and r_S form an LCR series resonance circuit. r_S , which mainly consists of the equivalent series resistance (ESR) of C_{IN} and the on-resistance of Q_1 , is negligibly small. Therefore, voltage spikes and ringing can be defined as resonance between C_P (C_{OSS} of Q_2) and L_P (wire inductance). The following subsections discuss an RC snubber that effectively suppresses this resonance phenomenon.

1.2. Voltage spike and ringing suppression using an RC snubber

As explained in Section 1.1, voltage spikes and ringing might be generated in a step-down converter at the turn-on of a switching device. This subsection describes an RC snubber, one of the measures used to protect against transient voltages.

A snubber is a protection circuit that suppresses transient voltages that are produced when a current is shut off. Snubbers are used to suppress voltage spikes caused by the switching of not only mechanical switches but also transistors and diodes. Snubbers protect not only switching devices but also other electronic parts and reduce switching noise. An RC snubber uses a resistor in series with a capacitor and is connected in parallel with a device that is subject to voltage spikes.

Figure 1.3 shows a simplified diagram of a step-down converter with an RC snubber. While an RC snubber suppresses voltage spikes and ringing produced by switching, the snubber resistor R_{SNB} causes a power loss during the charging and discharging of the snubber capacitor C_{SNB} . It is therefore necessary to select R_{SNB} and C_{SNB} , considering a trade-off between their voltage spike and ringing suppression effect and a power loss of R_{SNB} .

Figure 1.3 shows the charge/discharge path for the RC snubber. As described in (2) of Section 1.1, when Q_1 turns on, a spike voltage is induced across Q_2 with ringing. When this occurs, the spike voltage is charged into the snubber capacitor C_{SNB} via the path $V_{IN} \rightarrow Q_1 \rightarrow R_{SNB} \rightarrow C_{SNB}$. Therefore, the RC snubber helps reduce the peak spike voltage and ringing.

When Q_1 turns off, a current flows through L , C_{OUT} , and the body diode of Q_2 (as explained at Step 2 in (1) of Section 1.1). At the same time, the charge stored in the snubber capacitor C_{SNB} is discharged through the snubber-L- C_{OUT} loop (i.e., the discharge path shown in Figure 1.3(b)).

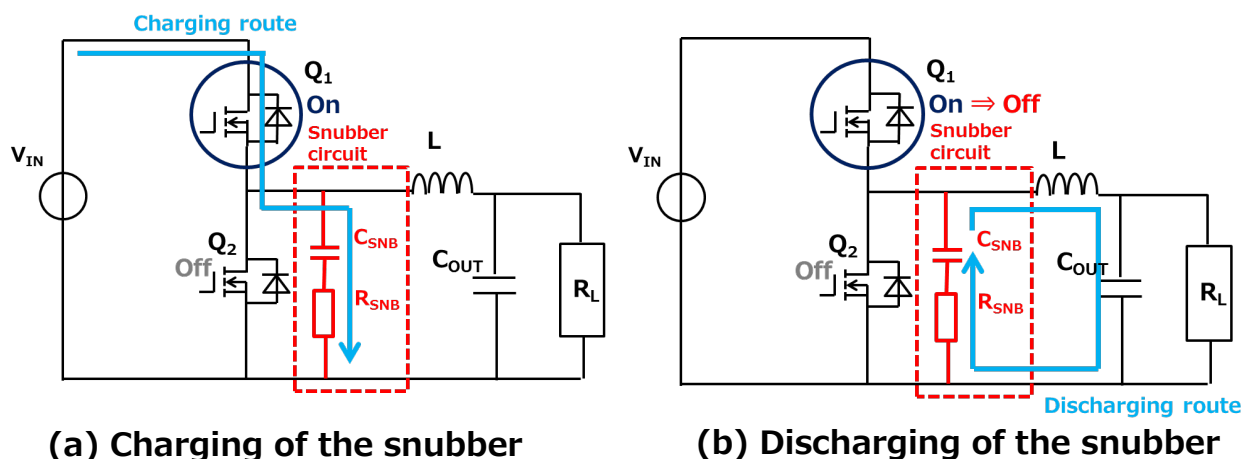


Figure 1.3 Snubber operation

1.3. Considering the snubber resistor and capacitor values

The resistor (R_{SNB}) and capacitor (C_{SNB}) values of an RC snubber are determined according to the resonance conditions (voltage spike and ringing) of the step-down converter.

a. Conditions of the resonant circuit

To determine the snubber resistor and capacitor values, it is necessary to consider the inductance and parasitic capacitance of the loop in which voltage spikes and ringing (resonance) occur as well as the ringing frequency as described below. The assumption is that ringing occurs through the equivalent circuit shown in Figure 1.2.

1) Ringing frequency (f_p)

The ringing frequency (f_p) is measured using the waveform of a step-down converter without a snubber.

(If the parasitic capacitance (C_p) and the stray inductance (L_p) are known, f_p can be calculated as $f_p = 1/(2\pi\sqrt{L_p C_p})$.)

2) Parasitic capacitance (C_p)

The parasitic capacitance (C_p) of the resonance loop is almost equal to the C_{OSS} of Q_2 . Read C_{OSS} at the input voltage (V_{in}) from a graph shown in the relevant MOSFET datasheet. (See Supplement A if the capacitance- V_{DS} curve is not shown in the datasheet.)

3) Parasitic inductance (L_p)

The parasitic inductance (L_p) can be calculated as follows from the parasitic capacitance (C_p) and the ringing frequency (f_p):

$$L_p = \frac{1}{(2\pi f_p)^2 \times C_p} \quad \text{Equation 1}$$

(See Supplement B.)

b. Snubber resistor (R_{SNB}) value

To maximize the positive effect of the snubber and minimize its negative effect (i.e., reflection from the snubber), the impedance of the snubber is generally matched to that of the circuit producing the ringing. For this purpose, use a snubber resistor (R_{SNB}) with a value equal or close to the characteristic impedance (Z) of the resonant circuit.

$$R_{\text{SNB}} = \text{characteristic impedance } Z = \sqrt{\frac{L_p}{C_p}} \quad \text{Equation 2}$$

(See Supplement C.)

If the ringing frequency (f_p) is known, the R_{SNB} value can be calculated as follows:

$$R_{\text{SNB}} = 1/(2\pi \times f_p \times C_p) = 2\pi \times f_p \times L_p \quad \text{Equation 3}$$

c. Snubber capacitor (C_{SNB}) value

A snubber capacitor (C_{SNB}) with a greater value has a more positive effect. However, there is a trade-off between the C_{SNB} value and a power loss^{*1} as described above. Generally, a snubber capacitor with a value one to four times the parasitic capacitance (C_p) is used, taking a power loss into consideration.

*1 Power loss caused by the RC snubber

When the charging and discharging of a snubber capacitor (C_{SNB}) complete within a switching period, the power loss of the RC snubber can be considered to be equal to the power dissipation of R_{SNB} due to charging and discharging. Hence:

$$P_{SNB} = (1/2 \times C_{SNB} \times V_{IN}^2 \times f_{SW}) \times 2 = C_{SNB} \times V_{IN}^2 \times f_{SW} \quad \text{Equation 4}$$

where P_{SNB} is the power loss of the RC snubber (dissipated by R_{SNB}) and f_{SW} is the switching frequency of the step-down converter.

If R_{SNB} is not connected to C_{SNB} , only an energy transfer occurs during the charging of C_{SNB} . In this case, the power loss is half the result of Equation 4 since no power is dissipated by R_{SNB} .

2. Verification of an RC snubber through simulation

This section simulates the voltage spikes and ringing of a step-down converter to verify the effect of an RC snubber.

It should be noted that the results of simulation might not exactly match the behavior of an actual circuit.

2.1. Voltage waveform of a step-down converter without a snubber

The 50 W step-down converter shown in Figure 2.1 has an input voltage (V_{IN}) of 12 V and an output voltage (V_{OUT}) of 5 V. It uses 30 V / 38 A products of the Toshiba U-MOSVIII-H series as a switching device. (Its switching frequency is 250 kHz.)

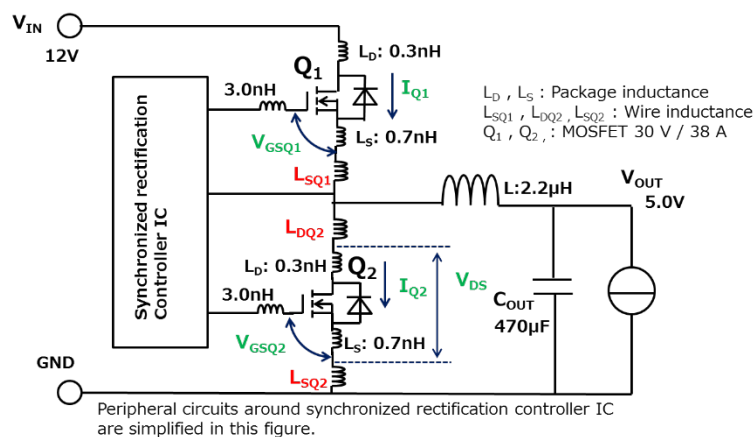


Figure 2.1 Step-down converter simulated

(1) Spike voltage and ringing

In Figure 2.1, when Q_1 turns on, the body diode of Q_2 transitions from the freewheeling mode to the reverse recovery mode. The drain-source voltage spike at Q_2 occurs because of the current slope (di/dt) of this transition and the inductance of the V_{IN} - Q_1 - Q_2 -GND loop. The magnitude of ringing voltage spikes is determined by the parasitic inductance and the capacitance (C_{OSS}) of Q_2 . The spike voltage increases with the increase in the parasitic inductance.

Figure 2.2 shows how the parasitic inductance affects spike voltage.

(a) In the absence of parasitic inductance: The V_{IN} - Q_1 - Q_2 -GND loop has zero inductance.

(b) In the presence of only MOSFET inductance: Only Q_1 and Q_2 have parasitic inductance. Wires have no inductance.

$$L_D = (0.3 \text{ nH} + L_S = 0.7 \text{ nH}) \text{ per MOSFET}$$

(c) In the presence of both MOSFET and wire inductances: Q_1 and Q_2 have parasitic inductance, and wires also have inductance.

$$(L_D = 0.3 \text{ nH} + L_S = 0.7 \text{ nH}) \text{ per MOSFET plus } L_{SQ1}, L_{DQ2}, \text{ and } L_{SQ2} (2 \text{ nH each})$$

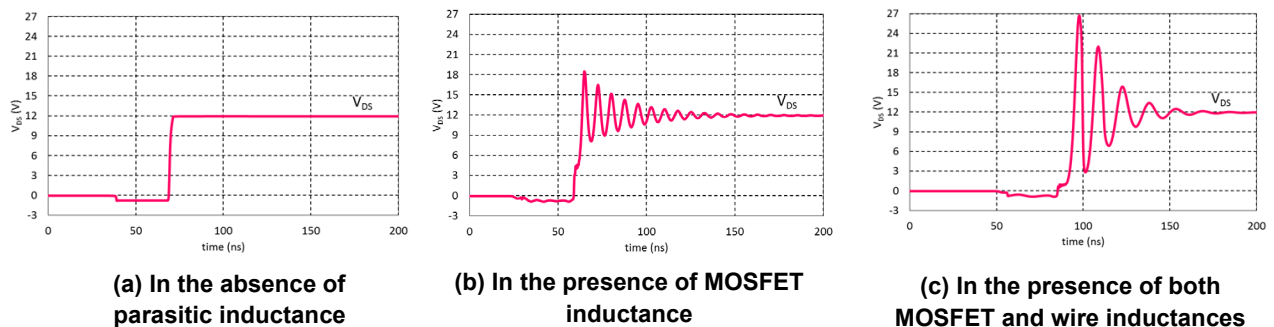


Figure 2.2 Results of Q_2 spike voltage simulation under different parasitic inductance conditions

(2) Mechanism of voltage spike generation

Figure 2.2(c) shows large voltage spikes. Figure 2.3 provides an enlarged view of voltage spikes to show their timing.

In Figure 2.1, when Q_1 turns on, the body diode of Q_2 transitions from the freewheeling mode to the reverse recovery mode. A change in current (di/dt) due to carrier recombination during reverse recovery and the inductance of the V_{IN} - Q_1 - Q_2 -GND loop cause a spike voltage (V_{Spike}) of $L \times di/dt$ (where L is the sum of MOSFET and wire inductances).

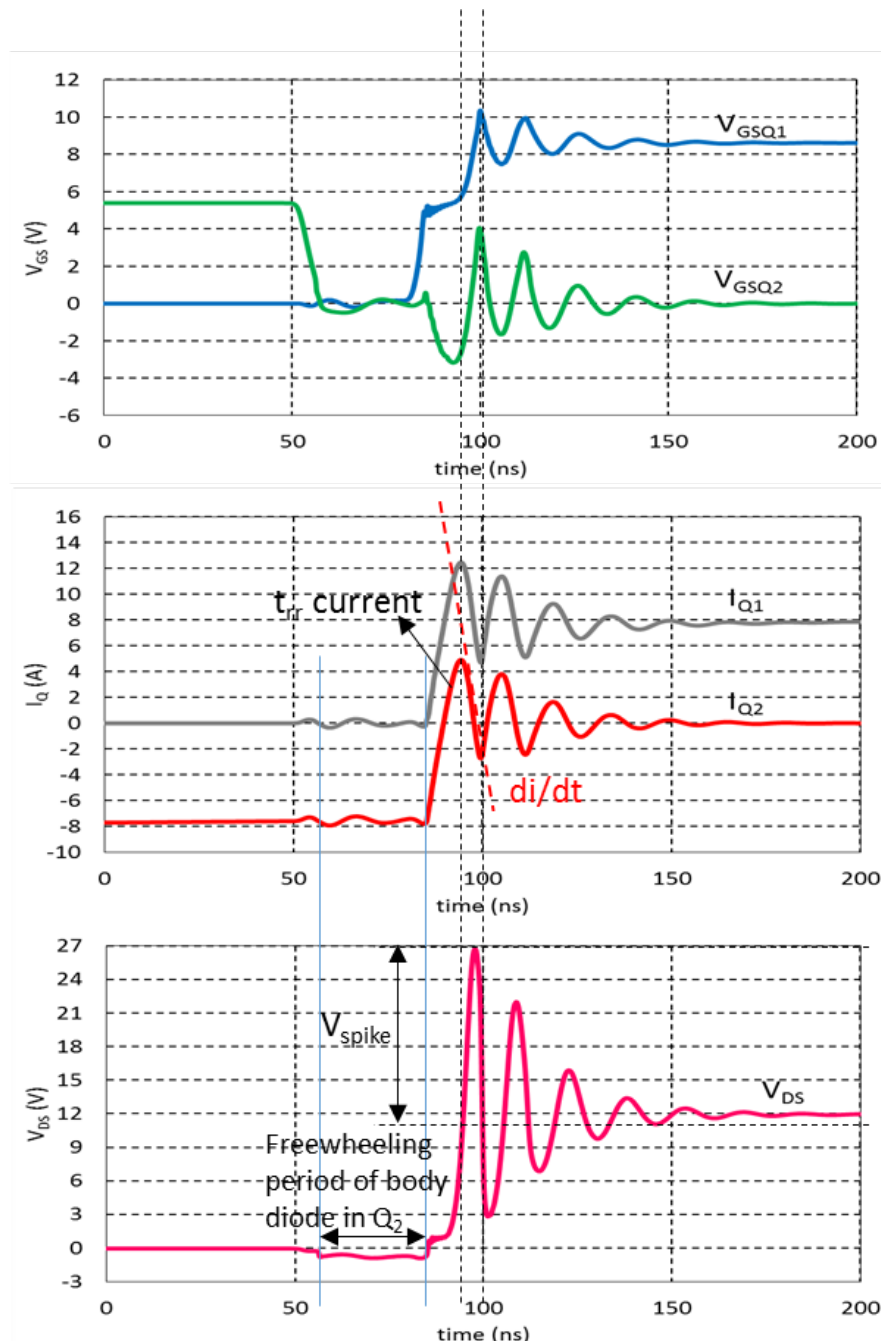


Figure 2.3 Enlarged view of Figure 2.2(c): Timing of voltage spike generation

2.2. Step-down converter with an RC snubber and its effect

2.2.1. RC snubber constants

Figure 2.4 shows the step-down converter with an RC snubber simulated. First, let's obtain the RC snubber constants.

For actual applications, the ringing waveform is observed in order to calculate the parasitic inductance and capacitance (Section 1.3.a). Here, suppose that the total parasitic inductance is 7 nH as shown in Figure 2.4 (not including the internal inductance ($L_D + L_S$) of the package of Q_2) and that the parasitic capacitance of the MOSFET is equal to C_{OSS} .

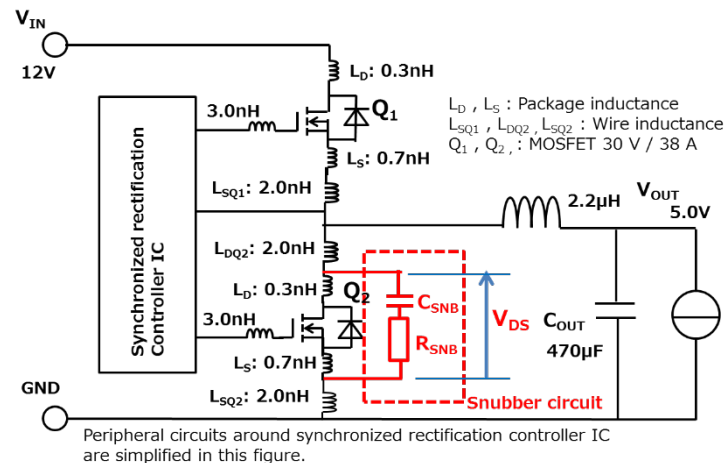


Figure 2.4 Step-down converter with an RC snubber

(1) Parasitic inductance (L_P) = 7 nH

(2) Parasitic capacitance (C_P)

The assumption is that C_P is equal to the C_{OSS} of Q_2 when the input voltage (V_{IN}) is applied. In this example, $V_{IN} = 12$ V. From the MOSFET datasheet, C_{OSS} ($=C_P$) is read as 650 pF at $V_{DS} = 12$ V (Figure 2.5).

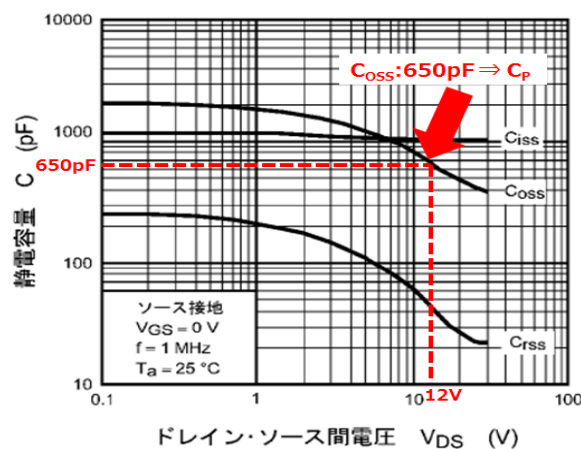


Figure 2.5 Reading C_P from the capacitance - V_{DS} curves

(3) Considering the snubber resistor (R_{SNB}) value

Based on the discussion of Section 1.3.b, let's use a snubber resistor (R_{SNB}) with a value equal to the characteristic impedance (Z) of the resonant circuit.

$$R_{SNB} = \text{characteristic impedance } Z = \sqrt{\frac{L_P}{C_P}}$$

Substituting 7 nH into L_P and 650 pF into C_P , R_{SNB} is calculated to be roughly 3.3 Ω .

(L_P does not include the internal inductance ($L_D + L_S$) of the package of Q_2 .)

(4) Considering the snubber capacitor (C_{SNB}) value

Generally, a snubber capacitor with a value one to four times the parasitic capacitance (C_P) is used. Let's use C_{SNB} with a capacitance of 650 pF as a reference point.

2.2.2. Effect of the RC snubber

Figure 2.6 shows the results of voltage spike simulation with different R_{SNB} and C_{SNB} values, including $R_{SNB}=3.3 \Omega$ and $C_{SNB}=650 \text{ pF}$ as reference points.

(1) Increasing C_{SNB} decreases spike and ringing voltages.

(2) Large R_{SNB} reduces the effect of the RC snubber whereas small R_{SNB} causes high-frequency oscillation. The optimal R_{SNB} value is close to the characteristic impedance of the resonant circuit.

As shown in Figure 2.6, an appropriate snubber reduces the spike voltage and the ringing settling time.

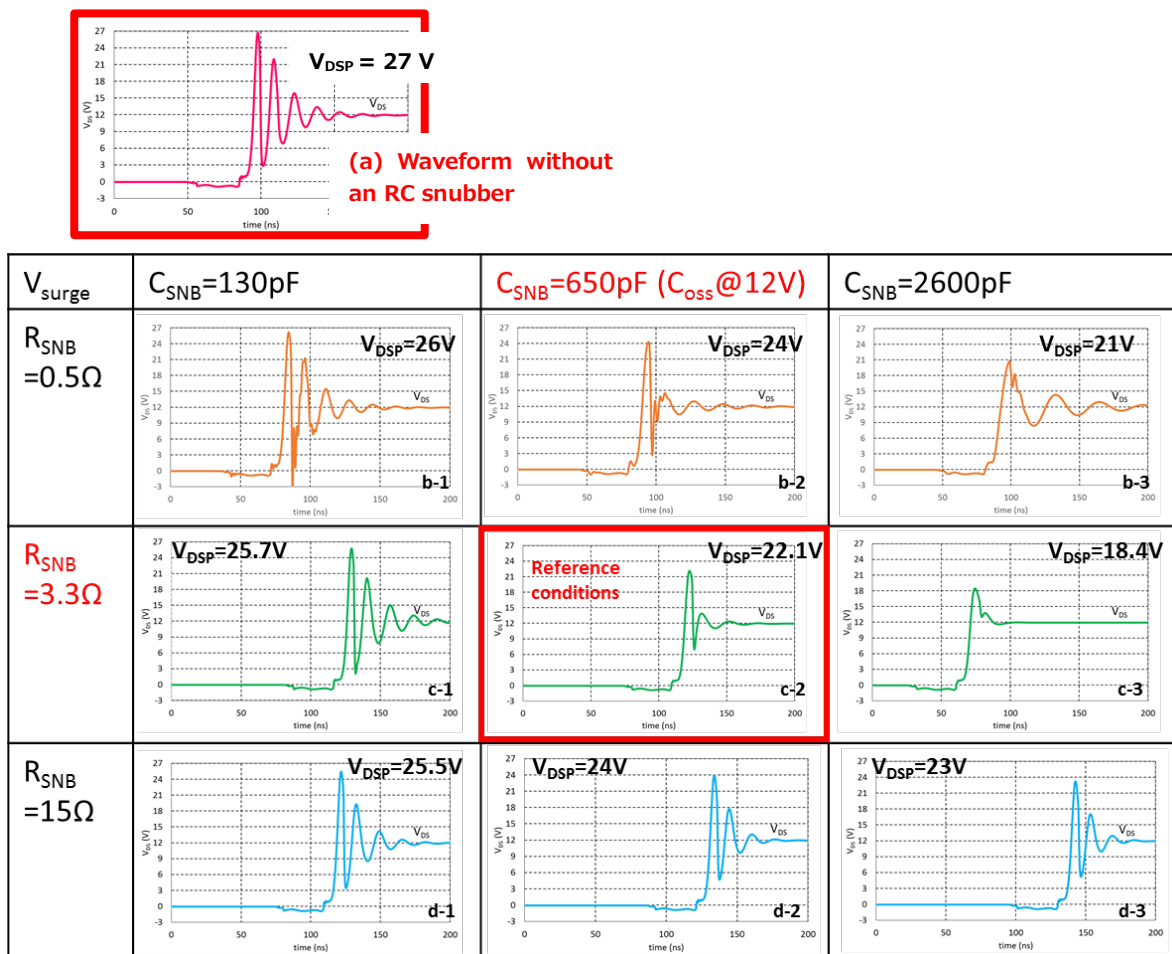


Figure 2.6 Q_2 spike voltage simulation: Effect of the RC snubber

2.2.3. Effect of the RC snubber on reducing the spike voltage

As described in (2) of Section 2.1, voltage spikes occur because of the di/dt during the carrier recombination period (t_{rr2}) of the reverse recovery current of the body diode and the parasitic inductance. Assuming that the parasitic inductance is constant, it is necessary to reduce the di/dt slope during t_{rr2} in order to reduce spike voltages. Figure 2.7 shows the differences in di/dt and spike voltage, depending on the presence or absence of an RC snubber. As the snubber charging current is added to the reverse recovery current, the step-down converter with an RC snubber has a shallower di/dt slope and consequently lower peak spike voltage. In Figure 2.7, V_{DSP} is as follows:

- Without a snubber:

$$V_{DSP} = 2.04 \text{ A/ns} \times 7 \text{ nH} + 12 \text{ V} = 26.3 \text{ V} \text{ (Simulation result: (a) in Figure 2.6, } V_{DSP} = 27 \text{ V)}$$

- RC snubber with a 3.3Ω resistor and a 650 pF capacitor:

$$V_{DSP} = 1.35 \text{ A/ns} \times 7 \text{ nH} + 12 \text{ V} = 21.5 \text{ V}$$

(Simulation result: (c-2) in Figure 2.6, $V_{DSP} = 22.1 \text{ V}$)

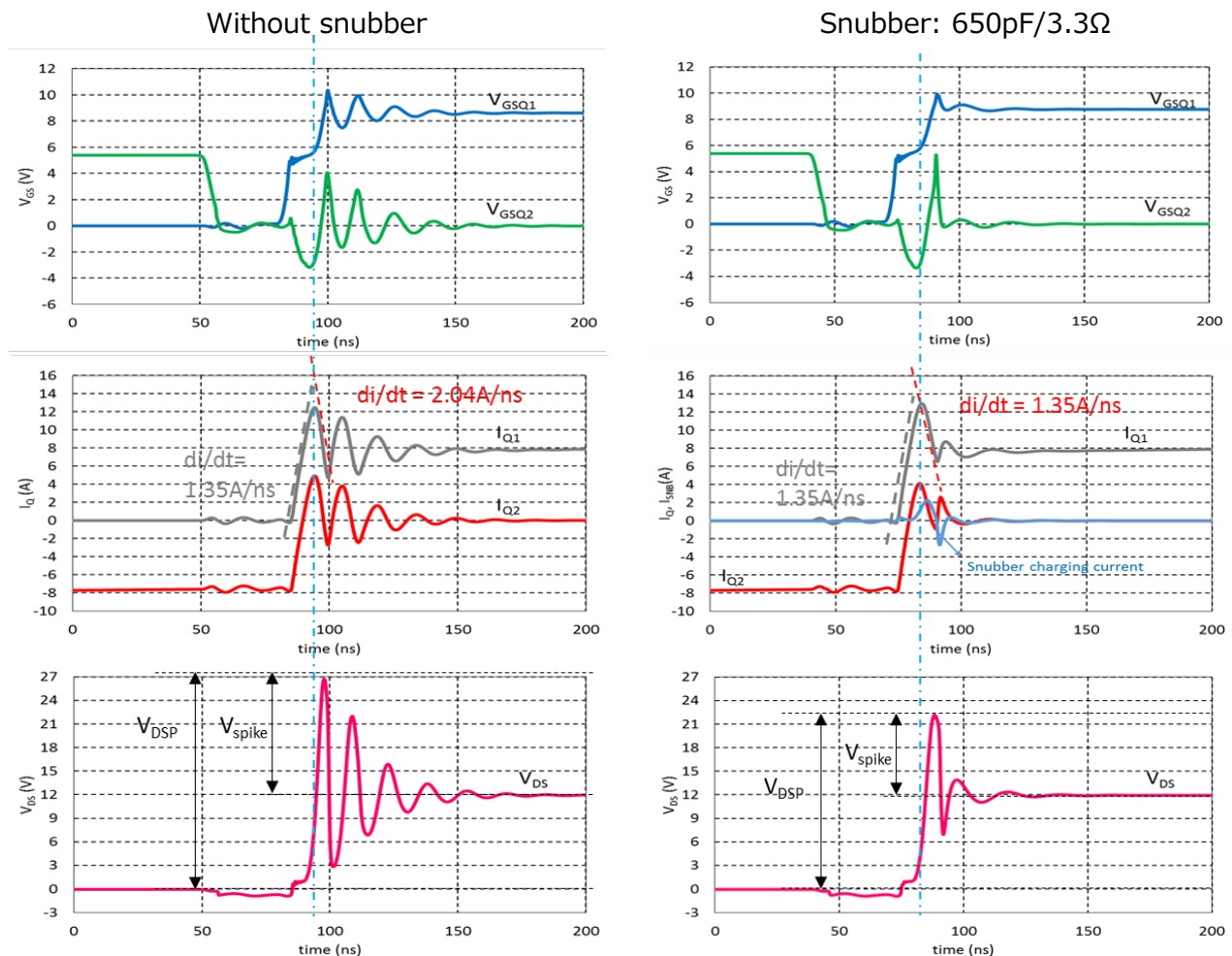


Figure 2.7 Q₂ spike voltage simulation: Difference due to the presence or absence of an RC snubber

3. Related information

To eliminate voltage spikes, it is important to minimize wire inductance. In the case of a step-down converter, it is also important to select appropriate MOSFETs and gate drive conditions in addition to using an RC snubber.

3.1. High-side MOSFET (Q_1)

(1) Reducing the turn-on speed of the high-side MOSFET (Q_1) helps suppress voltage spikes and ringing. The turn-on speed can be reduced by using a MOSFET with a large gate charge, particularly with a large gate switch charge^{*2} (Q_{sw}), or by using a large gate drive resistor (R_G). However, since there is a trade-off between the turn-on speed and the switching loss, it is also necessary to understand the voltage spike and power loss of the low-side MOSFET (Q_2).

*2 The amount of charge stored in the gate capacitance from when the gate-source voltage has reached V_{th} until the end of the Miller plateau, which affects the switching characteristics of a MOSFET

(2) Verification of the gate resistor (R_{GQ1}) for Q_1

Figure 3.2 compares the spike and ringing voltages generated when gate resistors (R_{GQ1}) of $0\ \Omega$ and $50\ \Omega$ are inserted to Q_1 gate of the step-down converter as shown in Figure 3.1. Inserting a larger gate resistor reduces the switching speed of Q_1 and makes the di/dt slope of the reverse recovery current shallower. Consequently, the peak spike voltage is reduced.

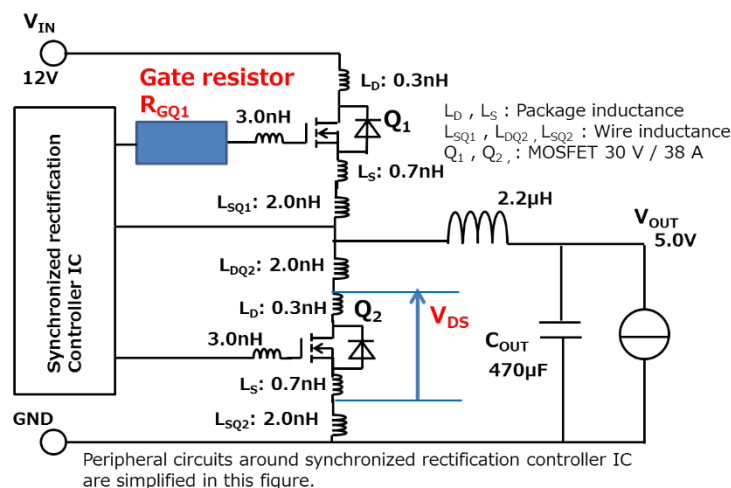


Figure 3.1 Gate drive resistors in a step-down converter

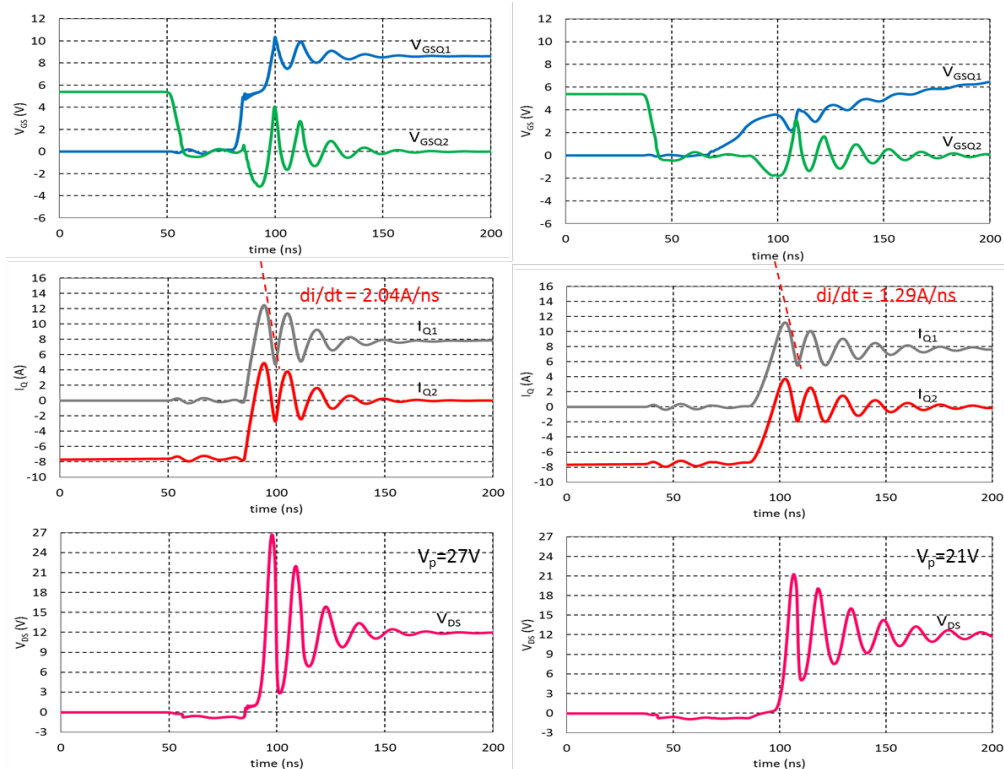


Figure 3.2 Q₂ spike voltage simulation: Difference according to the gate drive of the high-side MOSFET

3.2. Low-side MOSFET (Q₂)

The low-side MOSFET (Q₂) should have a body diode that provides soft recovery with small reverse recovery charge. Generally, low-voltage MOSFETs (with a V_{DS} of 60 to 100 V) exhibit soft recovery with small reverse recovery charge.

The MOSFETs of the Toshiba U-MOSVIII-H and U-MOSIX-H series incorporate an RC snubber and thus exhibit excellent characteristics.

Supplemental information

Supplement A: Calculating the MOSFET capacitance

If the datasheet of the low-side MOSFET does not show the C_{OSS} value at V_{IN} (input voltage), it can be measured in the following manners when designing a step-down converter.

Method 1

Connect a capacitor (C_{PO}) between the drain and source pins of the low-side MOSFET and find the C_{PO} value that halves the ringing frequency. The parasitic capacitance (C_p) of the low-side MOSFET is equal to one-third of C_{PO} :

$$C_p = C_{PO}/3$$

$f_p = 1/(2\pi\sqrt{LC})$ Hence, $(C_p + C_{PO})$ must be four times as large as C_p to reduce the ringing frequency by half.

$$(C_p + C_{PO}) = 4C_p$$

$$\text{Hence, } C_p = C_{PO}/3$$

Method 2

Measure the ringing frequency (f_p) from an actual waveform. Next, connect a capacitor (C_{PO}) between the drain and source pins of the low-side MOSFET and calculate the ringing frequency (f_{PO}). Let the ratio of f_p to f_{PO} be m . Since $f_p = 1/(2\pi\sqrt{L_P})$ and $f_{PO} = 1/(2\pi\sqrt{L_P(C_P + C_{PO})})$, C_P can be calculated as follows:

$$C_P = C_{PO}/(m^2 - 1)$$

Supplement B: Calculating parasitic inductance

If the parasitic capacitance (C_P) is unknown, the parasitic inductance (L_P) can be calculated as follows.

Measure the ringing frequency (f_p). Next, connect a capacitor (C_{PO}) between the drain and source pins of the low-side MOSFET and calculate the ringing frequency (f_{PO}).

f_p and f_{PO} are expressed by the following equations respectively:

$$f_p = \frac{1}{2\pi\sqrt{L_P C_P}}$$

$$f_{PO} = \frac{1}{2\pi\sqrt{L_P (C_P + C_{PO})}}$$

These equations can be restated as follows:

$$\frac{1}{f_p^2} = 4\pi^2 L_P C_P \quad \dots (A)$$

$$\frac{1}{f_{PO}^2} = 4\pi^2 L_P (C_P + C_{PO}) \quad \dots (B)$$

L_P can be calculated from the difference between A and B above.

$$\frac{1}{f_{PO}^2} - \frac{1}{f_p^2} = 4\pi^2 L_P C_{PO}$$

$$L_P = \frac{\frac{1}{f_{PO}^2} - \frac{1}{f_p^2}}{4\pi^2 C_{PO}}$$

Supplement C: Setting the snubber resistor value through impedance matching

To maximize the effect of an RC snubber and minimize the reflection from it, matching the impedance of the resonant circuit to that of the RC snubber (impedance matching^{*3}) is effective.

In this case, select a snubber resistor (R_{SNB}) with a value equal to the characteristic impedance.

Characteristic impedance $Z = \sqrt{\frac{L_P}{C_P}}$

Since $f_p = 1/(2\pi\sqrt{L_P C_P})$, the characteristic impedance can be expressed as:

- $Z = 1/(2\pi \times f_p \times C_P)$ or
- $Z = 2\pi \times f_p \times L_P$

In contrast, when an RC snubber is considered as a means of controlling ringing, the R_{SNB} value should be selected so that the output of the RLC resonant circuit decays at a rate (ζ) of one or greater.

When $C_{SNB} > C_p$, L_p , C_p , and R_{SNB} form a parallel resonant circuit. Therefore,

$$\text{Decay rate } (\zeta) = (1/2R_{SNB}) \times \sqrt{(L_p/C_p)}$$

When $\zeta \geq 1$,

$$R_{SNB} \leq (1/2) \times \sqrt{(L_p/C_p)}$$

Since the resonance loop might change depending on the position and magnitude of the parasitic inductance, care should be taken as to whether the RLC resonant circuit causes parallel or series resonance.

As a result of the foregoing, it is recommended to select an optimal snubber resistor with a value one-half to two times the characteristic impedance of the resonant circuit.

*3 Impedance matching

Impedance matching is the practice of matching the impedance of the source of a signal to that of the load to which it is transferred. The effects of impedance matching are as follows:

- 1) Let the source impedance and the load impedance in Figure 3.3 be R_S and R_L respectively.

Impedance matching maximizes the power consumption of the load

(i.e., power transfer to the load is the maximum when R_S and R_L have the same value.)

- 2) Signal reflection poses a problem in transferring a radio-frequency (RF) or high-speed pulse train.

Matching the source impedance to the load impedance minimizes signal reflection.

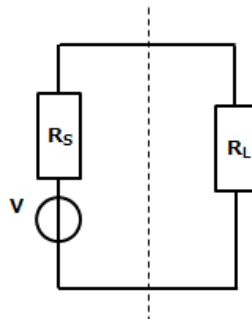


Figure 3.3 Impedance-matching circuit

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