

Impacts of the dv/dt Rate on MOSFETs

Description

A high dv/dt between the drain and source of the MOSFET may cause problems.
This document describes the cause of this phenomenon and its countermeasures.

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1. dv/dt rate of a MOSFET

dv/dt represents the rate of voltage change over time and is used to indicate the switching transient period of a MOSFET or the rate of change of its drain-source voltage caused by switching influence. An excessive dv/dt rate might cause false switching of, or permanent damage to, a MOSFET, depending on its usage conditions. The dv/dt capability is rated for some MOSFETs.

1.1. When a dv/dt ramp occurs

The dv/dt ramps that could affect normal operation of a MOSFET are as follows:

- ① The drain-source voltage exhibits a dv/dt ramp during switching transitions.
- ② Inverters and other circuits with an inductive load often use a pair of MOSFETs in a half-bridge configuration. The MOSFET drain-source voltage has a dv/dt ramp while its intrinsic body diode transitions from freewheel mode to reverse recovery mode

1.1.1. dv/dt ramp during switching transitions

The drain-source voltage of a MOSFET changes during the Miller plateau region of the switching transition. A change in the gate voltage causes a change in the drain current, which, in turn, causes a change in the drain potential and therefore a change in the gate-drain voltage v_{GD} . A reference to the dv/dt ramp of the MOSFET drain-source voltage means this V_{GD} change.

A gate-drain current of $C_{gd} \cdot dv_{GD}/dt$ flows while the drain-source voltage is changing in the Miller plateau region of the dv/dt period. In the Miller plateau region, a large capacitor is equivalently formed between the gate and GND. This capacitance is called the Miller capacitance. As the word “plateau” implies, the gate voltage does not increase during the Miller plateau region of the switching transition.

Figure 1.1 shows the switching circuit with an inductive load, and Figure 1.2 shows its waveforms. Most dv/dt problems occur with respect to an inductive load.

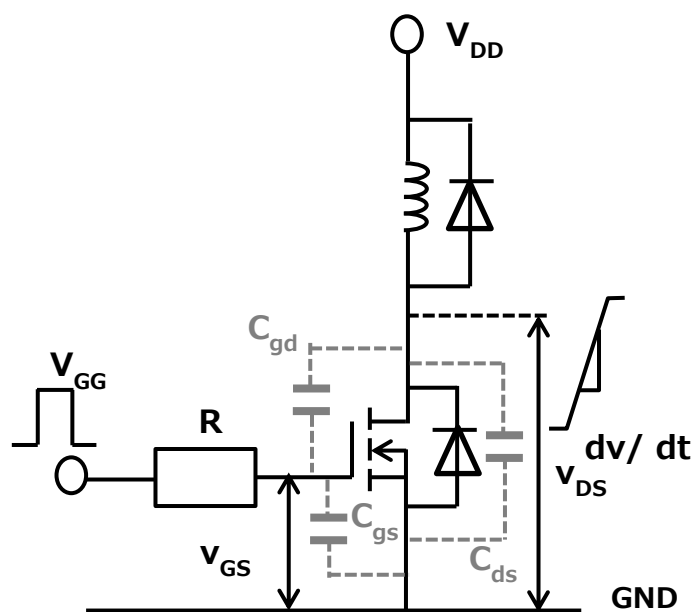


Figure 1.1 Switching circuit with an inductive load

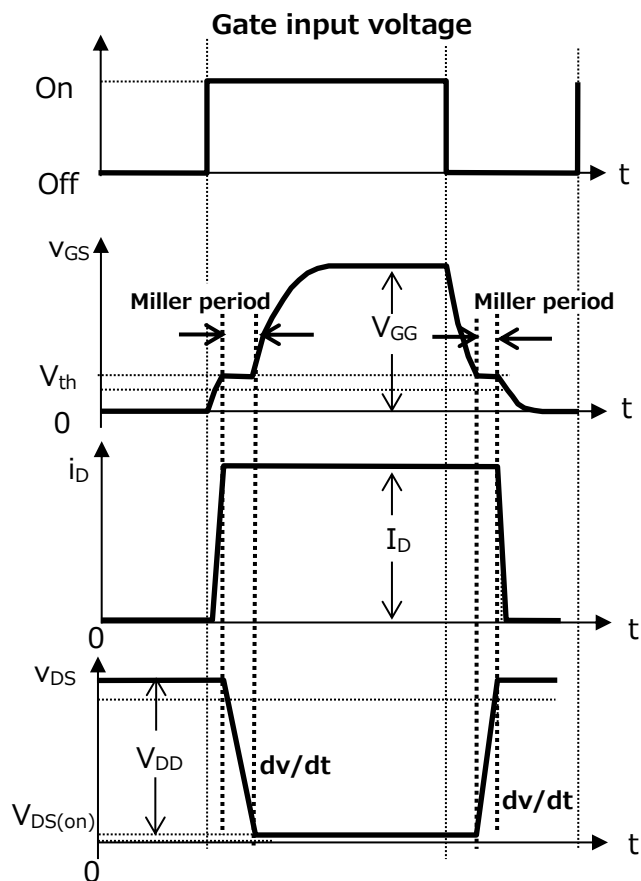


Figure 1.2 Switching waveforms of an inductive load

1.1.2. dv/dt ramp during the diode reverse recovery

When inverters and other circuits with an inductive load have a pair of MOSFETs in the upper and lower arms, a current flows through an intrinsic body diode during reverse recovery while they are switching. This section discusses the diode dv/dt during reverse recovery.

Suppose that an inductor current is flowing through the MOSFET Q_2 in Figure 1.3 and that Q_2 then turns off. When Q_2 turns off, the inductor current flows back through the body diode of Q_1 as a freewheel current I_F , shown by ① in Figure 1.3. At this time, the MOSFET Q_1 has a voltage equal to the forward voltage V_F across the body diode.

Next, when Q_2 turns on again, the current starts flowing through Q_2 as shown by ② in Figure 1.3, and the body diode of Q_1 enters reverse recovery, causing its drain-source voltage to rise sharply. The rate of change of the drain-source voltage equals the dv/dt rate of the body diode during reverse recovery. Figure 1.4 shows the waveforms of the body diode current and voltage.

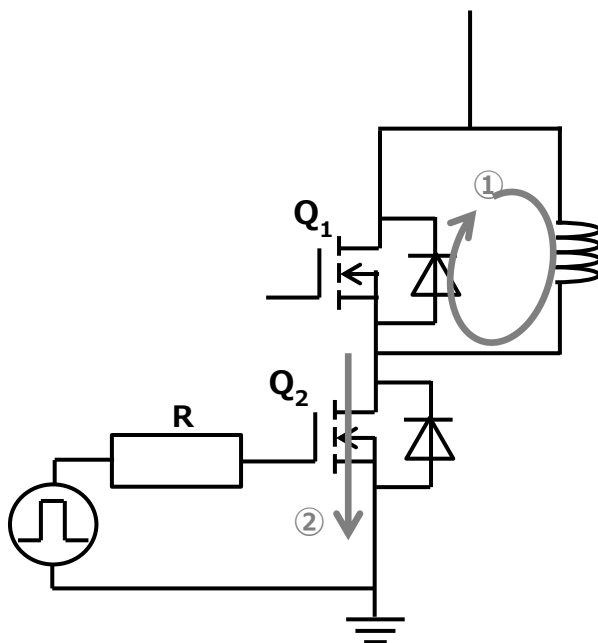


Figure 1.3 Switching of the upper and lower MOSFETs

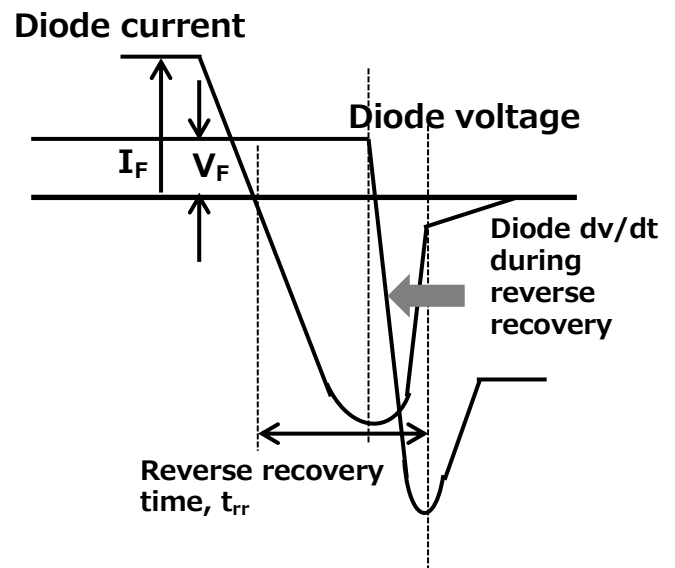


Figure 1.4 Diode reverse recovery waveforms

1.2. MOSFET switching operation (inductive load)

This section further discusses the switching operation of a MOSFET in Figure 1.1 during which its drain-source voltage has a dv/dt ramp.

This section focuses on a circuit with an inductive load. Note that its operation differs from that of a circuit with a resistive load. Here, the reverse recovery current of the freewheel diode in parallel with the inductor is also considered during the turn-on of the MOSFET.

1.2.1. Turn-on switching operation

Figure 1.5 shows the turn-on waveform of the circuit of Figure 1.1. The MOSFET has a dv/dt ramp during the period t_2 to t_3 (i.e., during the switching transition).

(1) 0 to t_1 (The MOSFET is in the off state.)

The gate voltage v_{GS} increases as a function of the gate resistance R , the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} :

$$v_{GS} = V_{GG} \{1 - \exp\{-t/[R(C_{gs} + C_{gd})]\}\} \quad \text{———— (1)}$$

(2) t_1 to t_2 (The MOSFET is switching.)

At t_1 , the gate voltage of the MOSFET exceeds its gate threshold voltage V_{th} , causing a current to start flowing in the drain. When the drain current i_D becomes equal to the load current I_O , i.e., the freewheel current, the freewheel diode in the forward-biased mode enters reverse recovery. i_D increases due to the reverse recovery current of the freewheel diode. During this period, the drain-source voltage v_{DS} of the MOSFET remains equal to V_{DD} and the gate voltage v_{GE} increase is almost the same as in the period from 0 to t_1 , which is expressed by Equation (1).

(3) t_2 to t_3 (The MOSFET is switching.)

As the reverse recovery current of the freewheel diode falls to zero, the drain current of the MOSFET reaches the load current I_O . Then, the gate voltage drops to V_{GS1} at which the drain current equals I_O . As the drain voltage decreases, the dv_{DS}/dt causes a current to flow through the gate-drain capacitance C_{gd} . This current is expressed as $i_{DG} = C_{gd} \cdot dv_{DS}/dt$. The dv_{DS}/dt rate is determined so that i_{DG} equals the current $(V_{GG} - V_{GS})/R$, which is a function of the gate pulse voltage V_{GG} and the gate resistance R .

During this period, the gate voltage v_{GS} remains almost constant at V_{GS1} . (Miller plateau)

(4) After t_3 (The MOSFET is in the on state.)

Because the drain-source voltage v_{DS} drops to almost zero at t_3 , the gate voltage begins to rise again due to R and $(C_{gs} + C_{gd})$.

The gate voltage is calculated as:

$$v_{GS} = [V_{GG} - V_{GS1}] \{1 - \exp[-(t - t_3) / R (C_{gs} + C_{gd})]\} + V_{GS1}$$

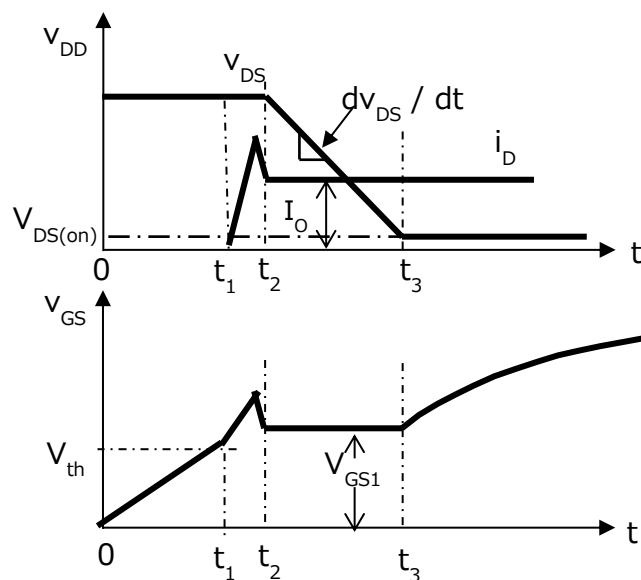


Figure 1.5 Turn-on curve

1.2.2. Turn-off switching operation

Figure 1.6 shows the turn-off waveform of the circuit of Figure 1.1. The MOSFET has a dv/dt ramp during the period t_2 to t_3 (i.e., during the switching transition).

(1) 0 to t_1 (The MOSFET is in the on state.)

The gate voltage v_{GS} decreases as a function of the gate resistance R , the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} :

$$v_{GS} = V_{GG} \cdot \exp\{-t / [R \cdot (C_{gs} + C_{gd})]\} \quad \text{————— (2)}$$

(2) t_1 to t_2 (The MOSFET is switching.)

When the gate voltage reaches V_{GS1} at which the drain current of the MOSFET reaches the load current I_O , the drain voltage begins to increase. As the drain voltage increases, the dv_{DS}/dt ramp causes a current to flow through the gate-drain capacitance C_{gd} . This current is expressed as $i_{DG} = C_{gd} \cdot dv_{DS}/dt$. The dv_{DS}/dt rate is determined so that i_{DG} equals the current v_{GS}/R , which is a function of the gate pulse voltage ($=0$ V) and the gate resistance R .

During the period t_1 to t_2 , the gate voltage v_{GS} remains almost constant at V_{GS1} , and the drain-source voltage v_{DS} of the MOSFET increases up to the supply voltage V_{DD} .

(3) t_2 to t_3 (The MOSFET is switching.)

When the drain-source voltage v_{DS} has reached the supply voltage V_{DD} , the freewheel diode goes into conduction. At the same time, the drain current i_D begins to decrease. Due to R and $(C_{gs} + C_{gd})$, the gate voltage v_{GS} begins to decrease again and continues to decrease until it reaches V_{th} . During this period, v_{GS} is expressed as: $V_{GS1} \cdot \exp\{-(t-t_2) / [R \cdot (C_{gs} + C_{gd})]\}$.

(4) After t_3 (The MOSFET is in the off state.)

Because the drain current i_D is zero, the drain-source voltage v_{DS} equals the supply voltage V_{DD} and dv_{DS}/dt is zero, the gate voltage begins to decrease again due to R and $(C_{gs} + C_{gd})$. During this period, v_{GS} is expressed as: $v_{GS} = V_{GS1} \cdot \exp\{-(t-t_2)/[R \cdot (C_{gs} + C_{gd})]\}$.

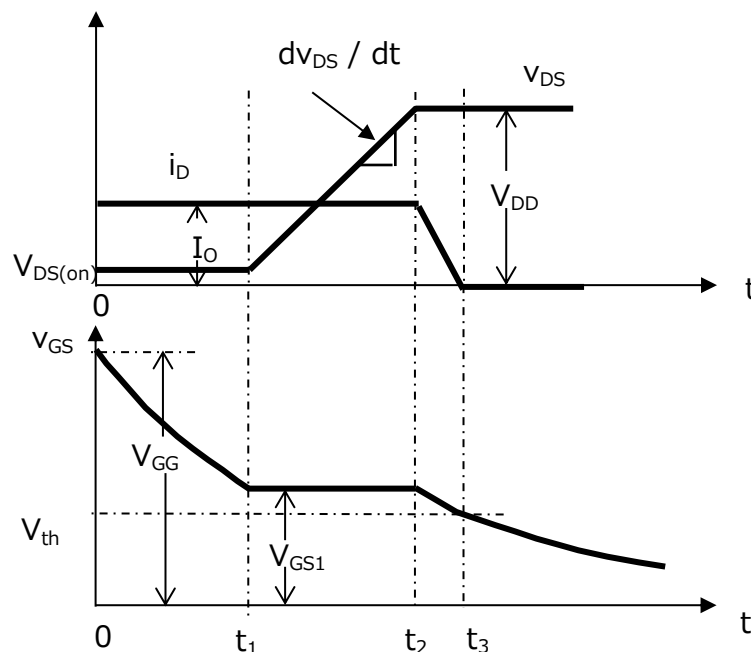


Figure 1.6 Turn-off curve

2. dv/dt problem

An excessive dv/dt rate might cause false switching, oscillation or permanent damage of a MOSFET. This section discusses these phenomena.

Figure 2.1 shows the cross section and equivalent circuit of a MOSFET.

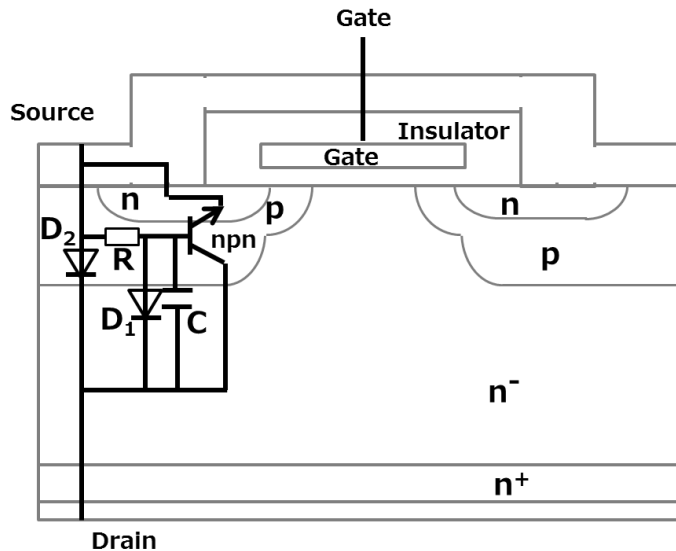


Figure 2.1 Cross section and equivalent circuit of a MOSFET

① dv/dt problem during switching

If the drain-source voltage changes rapidly during the turn-off of a MOSFET, its parasitic npn bipolar transistor might exhibit a false switching event (Figure 2.1), making the MOSFET vulnerable to secondary breakdown and permanent damage.

Upon turn-off, a high voltage surge generated by the wire stray inductance might cause the MOSFET to reach its avalanche breakdown voltage. A high dv/dt rate degrades the avalanche ruggedness of a MOSFET.

② dv/dt problem during the reverse recovery of the body diode

While the intrinsic body diode of a MOSFET is in reverse recovery, its drain-source voltage rises. This might falsely turn on the internal parasitic npn bipolar transistor, causing permanent damage to the MOSFET.

2.1. dv/dt problem during switching

2.1.1. False turn-on of the parasitic bipolar transistor due to a high dv/dt ramp

Figure 2.2 shows an equivalent circuit model for the turn-on of the parasitic npn bipolar transistor in a MOSFET due to a high dv/dt .

The drain-source voltage changes rapidly during turn-off of a MOSFET. The dv/dt in the drain-source voltage causes a varying current to flow through the pn junction capacitance C and resistance R . This current is expressed as:

$$i = C \cdot (dv/dt)$$

The current i causes a voltage drop ($i \times R$) across the resistor R , which is applied across the base and the emitter of the parasitic bipolar transistor. The parasitic bipolar transistor turns on if the voltage drop exceeds its base-emitter voltage to turn on.

The larger the dv/dt rate, the larger the current i and the larger the voltage across the base and the emitter becomes. The larger base-emitter voltage makes the parasitic npn bipolar transistor more susceptible to false turn-on.

At this time, if the drain-source voltage v_{DS} of the MOSFET is high, the parasitic npn transistor might enter secondary breakdown, causing permanent damage to the MOSFET.

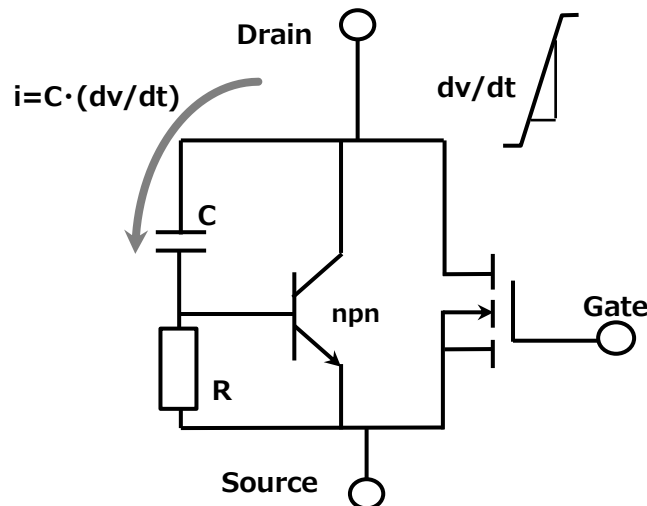


Figure 2.2 Equivalent circuit for false turn-on of the parasitic npn bipolar transistor

2.1.2. dv/dt versus avalanche ruggedness

A MOSFET with a high switching speed has high dv/dt and di/dt rates. The di/dt ramp during the turn-off of the MOSFET causes a voltage surge v due to the circuit stray inductance:

$$v = L \cdot di/dt$$

In some cases, the surge voltage may cause excessive noise or oscillation of the MOSFET.

In the event of an excessive surge voltage, the MOSFET may also exceed its rated voltage and enter the avalanche region. At this time, an avalanche current passes through the MOSFET. An avalanche current exceeding the current or energy limit might cause permanent damage to the MOSFET.

Avalanche behavior:

Avalanche breakdown occurs in the following two modes. Figure 2.3 shows a test circuit for avalanche behavior, and Figure 2.4 gives an equivalent circuit model for an avalanche current. Figure 2.5 shows its waveform.

(A) Avalanche current breakdown

If a voltage higher than the breakdown voltage is applied across the drain and the source, an avalanche current i flows in the reverse direction of the diode and to the resistor R , as shown in the equivalent circuit of Figure 2.4. As a result, a forward voltage, $i \times R$, appears across the base and the emitter of the transistor.

If this voltage exceeds the base-emitter voltage to turn on, the parasitic npn transistor turns on, causing a current to flow through the transistor. At this time, if the drain-source voltage is high, the parasitic npn transistor might enter secondary breakdown, causing permanent damage to the MOSFET.

(B) Avalanche energy breakdown

If avalanche behavior causes a MOSFET to enter the breakdown voltage BV_{DSS} region, a current continues flowing from the drain to the source of the MOSFET until the energy stored in the inductive load at the drain is consumed. Because of this current and voltage BV_{DSS} , a power loss occurs. The resulting energy causes the device temperature to increase, and causes permanent damage to the device if it exceeds the rated channel temperature.

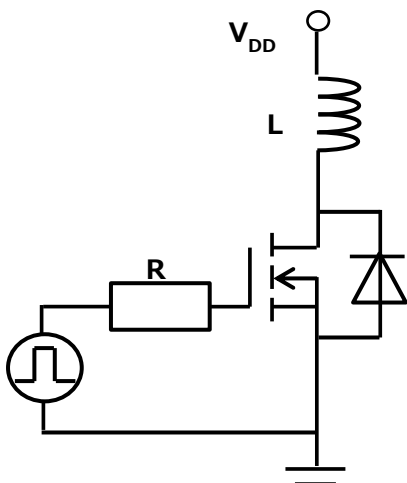


Figure 2.3 Test circuit for avalanche behavior

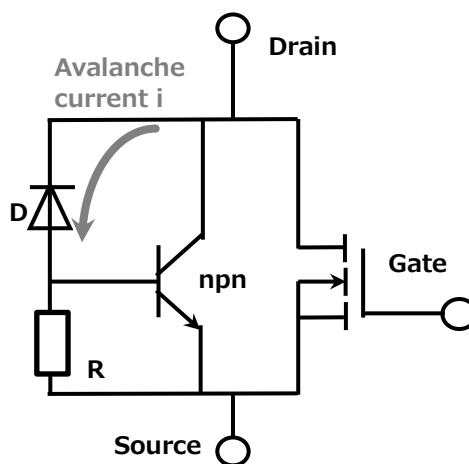


Figure 2.4 Equivalent circuit model for avalanche behavior

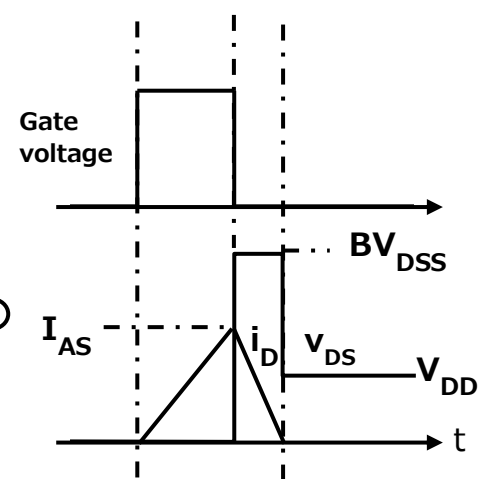


Figure 2.5 Waveform of the equivalent circuit

2.2. dv/dt problem for a MOSFET in the off state (e.g., during reverse recovery of the body diode)

2.2.1. False turn-on of the parasitic bipolar transistor caused by the dv/dt of the diode reverse recovery

For example, suppose that an inverter circuit with an inductive load has MOSFETs in the upper and lower arms. The intrinsic body diode allows a freewheel current to pass through a MOSFET. A recovery current flows through the body diode when it transitions from freewheeling mode to reverse recovery mode. In reverse recovery mode, the drain-source voltage of the MOSFET rises. The diode's recovery current and recovery dv/dt might cause false turn-on of the parasitic npn bipolar transistor and permanent damage to the MOSFET.

Figure 2.6 shows an equivalent circuit of a MOSFET. A voltage change dv/dt causes a current, $i = C \cdot (dv/dt)$, to flow to the capacitance C of the pn junction between the drain and the gate. This causes a voltage drop of $i \cdot R$ across the resistor R . If the voltage drop exceeds the base-emitter voltage to turn on, the parasitic npn transistor turns on. At this time, if the drain-source voltage v_{DS} is high, the parasitic npn transistor might enter secondary breakdown. As is the case in the situation described in **Section 2.1.1, "False turn-on of the parasitic bipolar transistor due to a high dv/dt ramp,"** the MOSFET might be permanently damaged, although the failure mode is different.

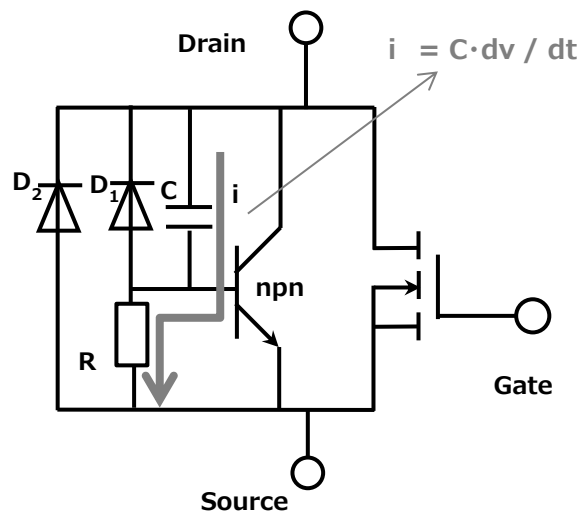


Figure 2.6 Equivalent circuit model during the dv/dt

2.2.2. Self-turn-on phenomenon due to dv/dt

For example, inverter and non-isolated synchronous rectification converter circuits consist of a bridge using MOSFETs. When multiple MOSFETs switch at high speed, a fast rising voltage is applied across the drain and source terminals of the MOSFET in the off state. Depending on the voltage change over time dv/dt , an excessive voltage is induced at the gate input of the MOSFET according to the ratio between its gate-drain capacitance C_{gd} and gate-source capacitance C_{gs} or a current flowing to the gate resistor R via C_{gs} . An excessive gate voltage causes self-turn-on of a MOSFET.

When a voltage with a dv/dt ramp is applied to a MOSFET, a current flows through its gate-drain capacitance C_{gd} . A theory of operation is omitted here.

$$i = C_{gd} \frac{dv}{dt}$$

The gate-drain current, in turn, generates a voltage across the gate and source terminals:

$$v_{GS} = RC_{gd} \frac{dv}{dt} \left\{ 1 - \exp\left(\frac{-t}{(C_{gs} + C_{gd})R}\right) \right\} \dots \dots \dots (2)$$

(Here, the assumption is that MOSFET capacitances, C_{gs} and C_{gd} , do not change with the voltage.)

In the time region $t \ll (C_{gs} + C_{gd}) \cdot R$, a gate voltage, $v_{GS} \approx \frac{C_{gd}}{(C_{gs} + C_{gd})} v(t)$, is induced according to the ratio between C_{gs} and C_{gd} .

In the time region $t \gg (C_{gs} + C_{gd}) \cdot R$, a gate voltage is induced according to the product of a current flowing through the gate-drain capacitance C_{gd} , $i = C_{gd} \frac{dv}{dt}$, and the gate resistance R .

The following shows an example of simulation results, illustrating a self-turn-on phenomenon due to a dv/dt and a gate resistor. Figure 2.7 shows a test circuit. If Q_2 turns on while the body diode of Q_1 is in freewheeling mode, the body diode of Q_1 enters reverse recovery mode, causing a rise in the voltage dv/dt of Q_1 . The dv/dt current flows to the gate of Q_1 . As a result, a voltage that appears across the gate resistor causes self-turn-on of Q_1 . Figure 2.8 shows a waveform with self-turn-on. Note that a large gate resistor was chosen to force self-turn-on to occur.

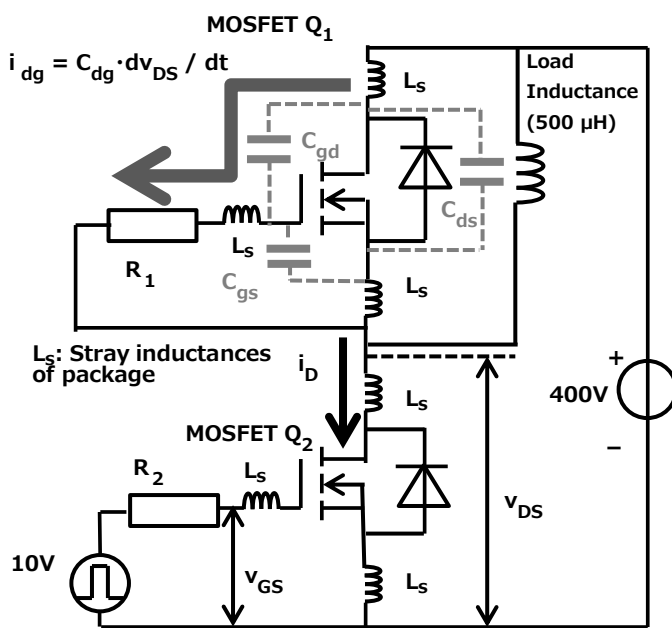


Figure 2.7 Test circuit for self-turn-on

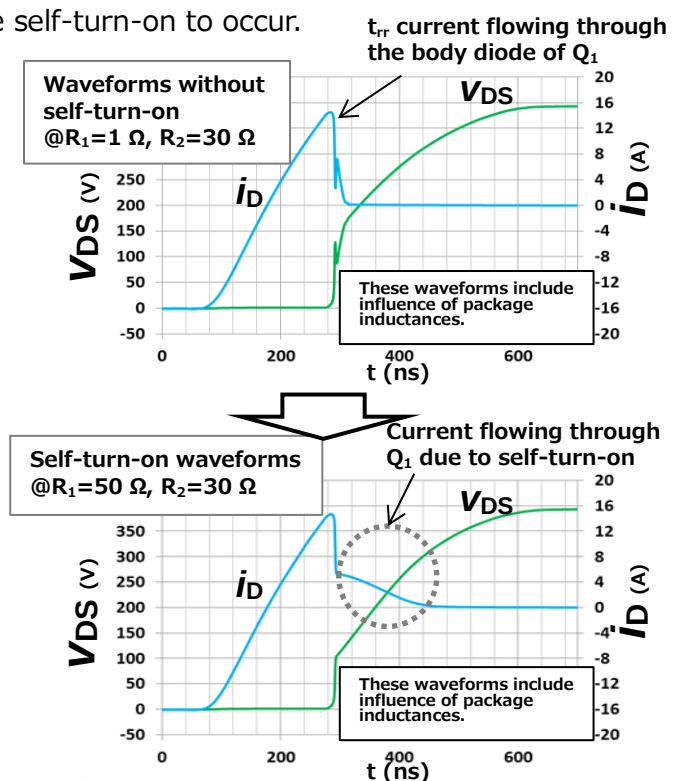


Figure 2.8 Self-turn-on waveform

To prevent self-turn-on, a capacitor can also be added between the gate and source terminals of a MOSFET as shown in Figure 2.9. Note, however, that the capacitor affects the switching speed of the MOSFET.

Figure 2.10 shows the improved waveform compared to the waveform in Figure 2.8 due to the addition of the gate-source capacitor.

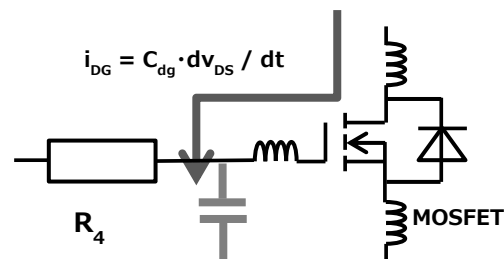


Figure 2.9 Adding a capacitor across the gate and source terminals

Improved self-turn-on waveform

@ $R_1=50\Omega$, $R_2=30\Omega$, Gate-source capacitance $C=3000$ pF

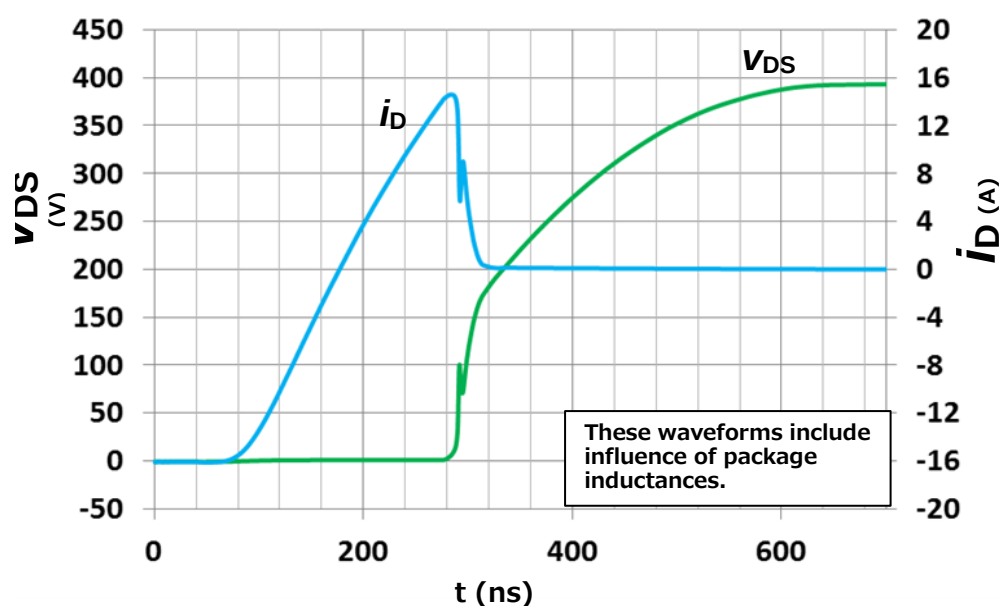


Figure 2.10 Improved self-turn-on waveform

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