

**DC 300 V Input BLDC Motor
Sensorless Control Circuit
Using TPD4164F**

Design Guide

RD179b-DGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

1. Introduction.....	3
2. Components Used	4
2.1. Microcontroller TMPM374FWUG.....	4
2.2. Intelligent Power Device TPD4204F.....	5
3. Circuit Design.....	6
3.1. MCU Peripheral Circuit	7
3.2. Motor Drive Circuit.....	9
3.3. Shunt Current Measurement Circuit.....	10
3.4. Error Detection Circuit	11
3.5. Motor Voltage Detection Circuit	12

1. Introduction

This Design Guide (hereinafter referred to as this Guide) describes the designs of DC 300 V Input BLDC Motor Sensorless Control circuit (hereinafter referred to as this reference design).

In this reference design, [TMPM374FWUG](#) microcontroller is used as motor controller, and vector control without sensor is realized. An intelligent power device for a three-phase inverter, which contains switching element and gate driver in a small package is used as motor driver. The intelligent power device used in this design (RD179-1) is as follows:

- [TPD4164F](#) (built-in IGBT type, 600 V withstand voltage, 2.0 A maximum output current, and HSSOP31 package).

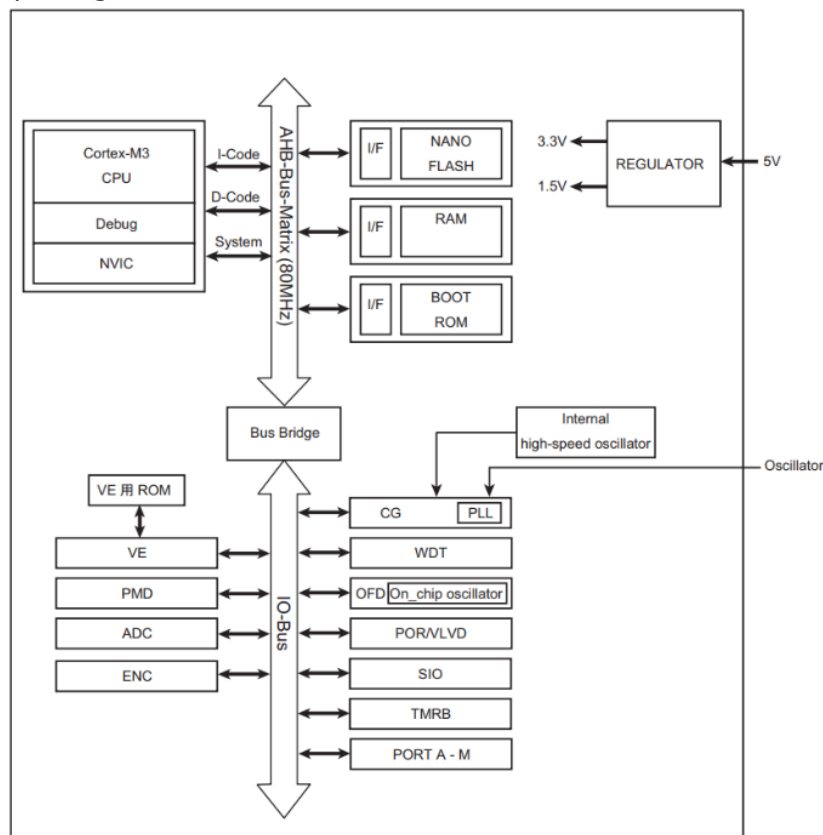
2. Components Used

2.1. Microcontroller TPM374FWUG

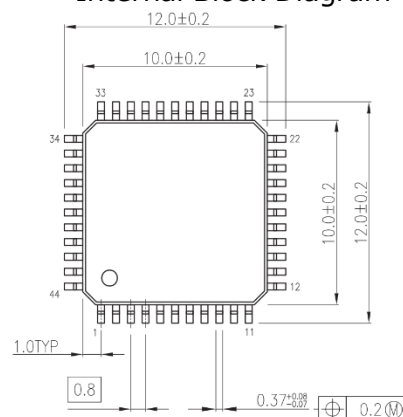
This reference uses the Toshiba microcontroller [TPM374FWUG](#) for controlling the motor.

The main features of TPM374FWUG are as follows:

- Equipped with high-speed Arm Cortex-M3 and which can operate up to 80 MHz (operating temp. range -40 to 80 °C)
- Equipped with functions suitable for motor control such as A/D converter, programmable motor driver, vector engine, and encoder
- Supports 5 V voltage operation
- Small LQFP44 package



Internal Block Diagram

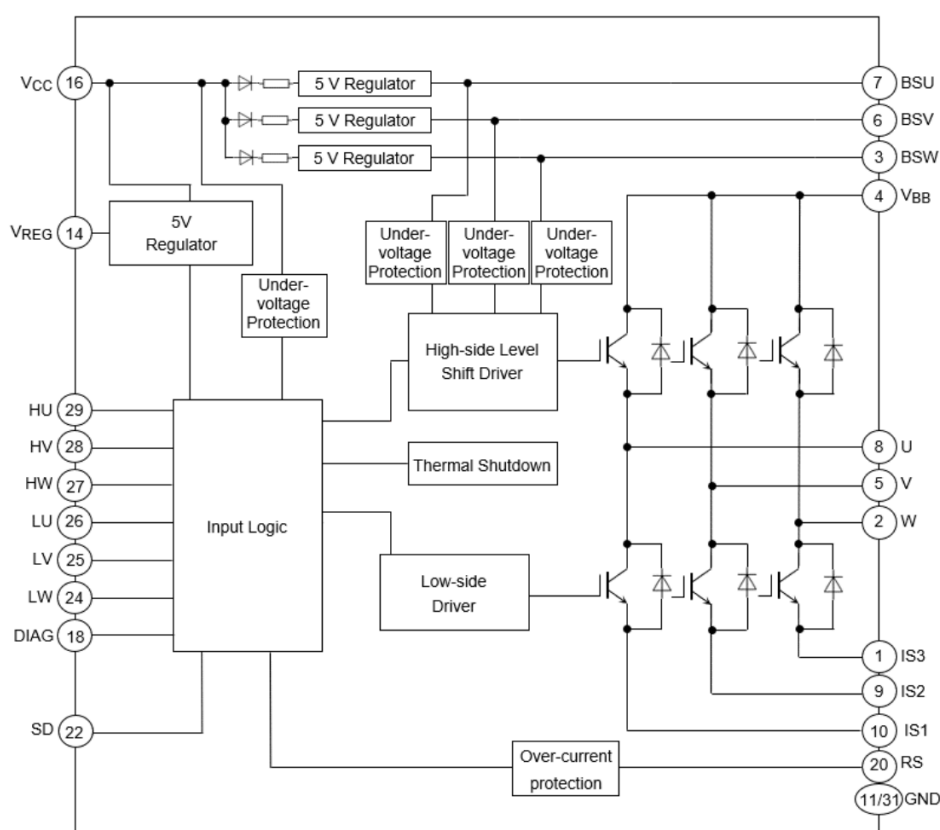


LQFP44 Package

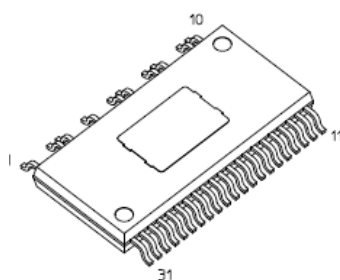
2.2. Intelligent Power Device TPD4204F

This reference (RD179-1) uses the Intelligent Power Device [TPD4164F](#). TPD4164F is a high-voltage, three-phase brushless motor driver with a built-in IGBT rated at 600 V, and supports 3-shunt resistor current sensing. It also incorporates level-shifted high-side driver, low-side driver, overheat protection circuit, under-voltage protection circuit, overcurrent protection, shutdown (SD) function. Therefore, a three-phase brushless motor can be driven directly by taking control signal input from a microcontroller. The main features are as follows.

- Output tolerance V_{BB} 600 V (Max.)
- Current I_{out} 2.0 A (Max.)
- HSSOP31 package



Internal Block Diagram



HSSOP31 Package

3. Circuit Design

This section explains the main points of circuit design. Refer to RD179-SCHEMATIC1 for the schematics and to RD179-BOM1 for the bill of materials.

Fig. 3.1 shows the block diagram of this reference.

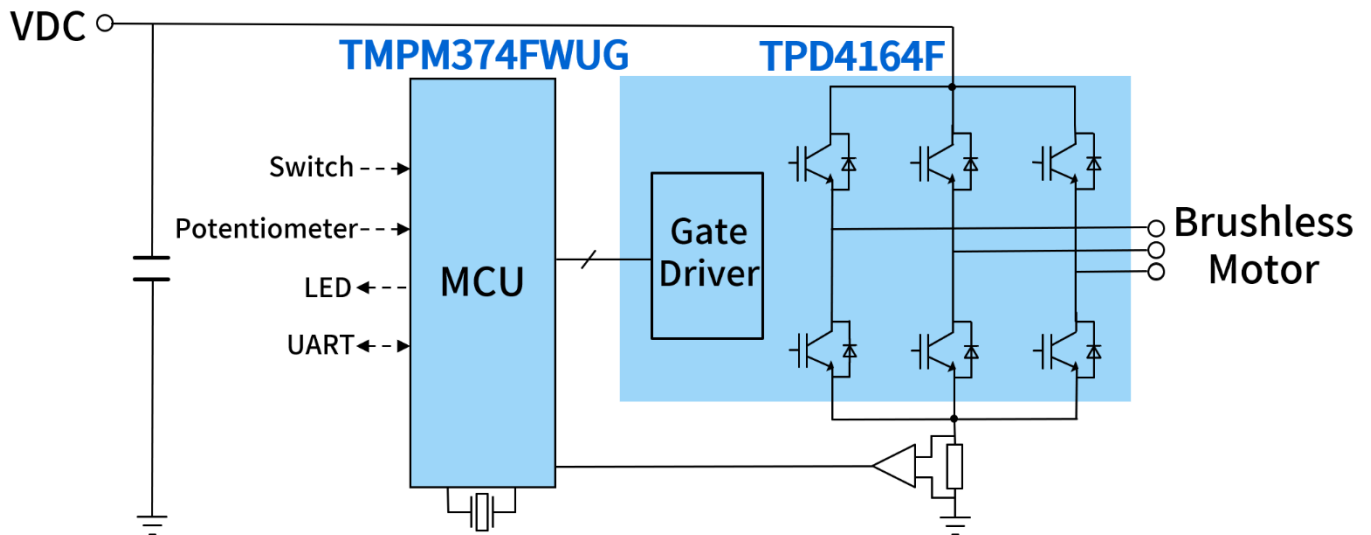


Fig. 3.1 Block Diagram of DC 300 V Input BLDC Motor Sensorless Control Circuit

3.1. MCU Peripheral Circuit

Fig. 3.2 shows the MCU peripheral circuit.

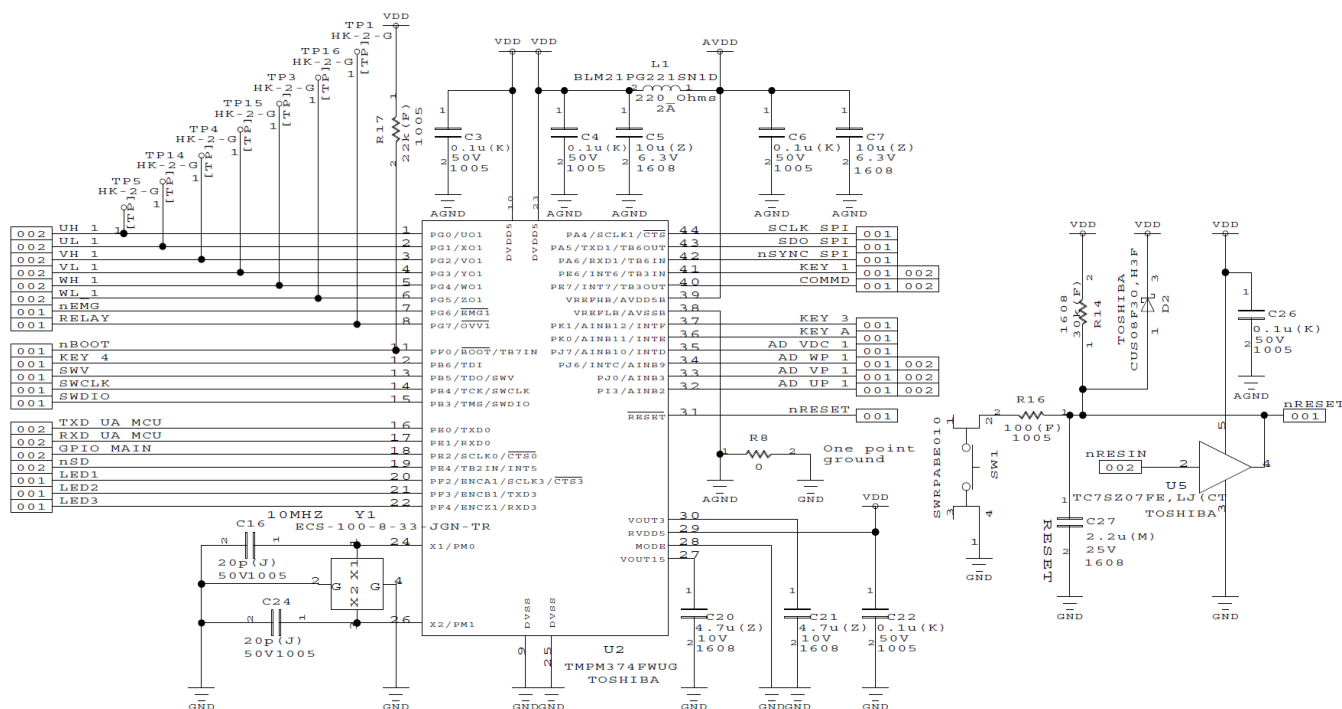


Fig. 3.2 MCU Peripheral Circuit

VDD (5 V) connected from the control power input terminal (J10) is supplied to the digital power supply used in MCU, etc. Bypass capacitors (C3, C4, C5, etc.) are required to eliminate power supply noise, etc. The 5 V analogue power supply (AVDD) of this reference design is generated from the 5V control power supply (VDD) and is received from the control power supply input pin (J10) via the ferrite bead (L1). The ground (GND) of the control power supply is connected to the ground (AGND) of the analogue power supply at a single point. VOUT3 pin (pin 30) and VOUT15 pin (pin 27) of the MCU must have the same capacitance of 3.3 to 4.7 μ F as the stabilizing capacitor of the power supply in the MCU. This reference design uses a 4.7 μ F capacitor for C20 and C21.

The capacitance of the load capacitors (C16 and C24) used in the resonator circuit of the microcontroller is selected so that the sum of equivalent capacitances of these capacitors in series (C16, C24), and the capacitance of resonator circuit in the MCU, and the pattern capacitance (approximately 10 pF) becomes the load capacitance of the resonator (X1). Since the load capacitance of the resonator (crystal resonator) used in this reference is 20 pF (Typ.), the capacitance of C16 and C24 is set to be 20 pF. The patterns to the resonator (X1) and the capacitors (C20 and C21) connected from the MCU should be as short as possible, and consideration should be given to minimizing the effect of noise on the surrounding signals. The 10 MHz clock generated by the crystal resonator circuit is used by the internal PLL to generate a system clock of up to 80 MHz.

The reset signal (nRESET) to the MCU is generated by the logical OR of the push switch (S1) and the external reset signal (nRESIN).

Each pin of the MCU is multiplexed, and the pin assignment is decided by the software setting. Table 3.1 lists the pin assignments used in this reference design. The function of each pin used in this reference is indicated by orange color.

Table 3.1 MCU Pin Assignment

Pin Number	Functions				Direction	Description
1	PG0	UO1			Out	U-phase high-side switch
2	PG1	XO1			Out	U-phase low-side switch
3	PG2	V01			Out	V-phase high-side switch
4	PG3	YO1			Out	V-phase low-side switch
5	PG4	WO1			Out	W-phase high-side switch
6	PG5	ZO1			Out	W-phase low-side switch
7	PG6	EMG1#			In	Emergency signal input
8	PG7	OVV1#			Out	GPIO-Relay control (not used)
9	DVSS				-	GND
10	DVDD5				-	Digital power (5 V)
11	PF0	BOOT#	TB7IN		In	Boot mode (usually connected to ground)
12	PB6	TDI			In	GPIO-S SW4 (not Used)
13	PB5	TDO	SWV		In/Out	SWD-SWV
14	PB4	TCK	SWCLK		Out	SWD-SWCLK
15	PB3	TMS	SWDIO		In/Out	SWD-SWDIO
15	PE0	TXD0			Out	UART-TXD0 (for host communication)
17	PE1	RXD0			In	UART-RXD0 (for host communication)
18	PE2	SCLK0	CTS0#		In/Out	GPIO-Reserved (for host communication)
19	PE4	TB2IN	INT5		Out	GPIO-IPD Shutdown (not used)
20	PF2	ENCA1	SCLK3	CTS3#	Out	GPIO-LED1
21	PF3	ENCB1	TXD3		Out	GPIO-LED2
22	PF4	ENCZ1	RXD3		Out	GPIO-LED3
23	DVDD5				-	Digital power (5 V)
24	PM0	X1			-	10 MHz resonator
25	DVSS				-	GND
26	PM1	X2			-	10 MHz resonator
27	VOUT15				-	(Connected to capacitor)
28	MODE				In	(Connected to GND)
29	RVDD5				-	Digital power (5 V)
30	VOUT3				-	(Connected to capacitor)
31	RESET#				In	Reset
32	PI3	AINB2			Analog In	U-phase shunt current
33	PJ0	AINB3			Analog In	V-phase shunt current
34	PJ6	AINB9	INTC		Analog In	W-phase shunt current
35	PJ7	AINB10	INTD		Analog In	Inverter DC bus voltage
36	PK0	AINB11	INTE		Analog In	Voltage of Potentiometer(VR1)
37	PK1	AINB12	INTF		In	GPIO-S SW3 (for CW-CCW switch)
38	AVSSB/VREFLB				-	Analog GND
39	AVDD5B/VREFHB				-	Analog power (5 V)
40	PE7	TB3OUT	INT7		In	GPIO-S SW2 (for host communication)
41	PE6	TB3IN	INT6		In	GPIO-S SW1 (not used)
42	PA6	TB6IN	RXD1		Out	SYNC# for external DAC
43	PA5	TB6OUT	TXD1		Out	SDO for external DAC
44	PA4	CTS1#	SCLK1		Out	SCLK for external DAC

3.2. Motor Drive Circuit

Fig. 3.3 shows the motor drive circuit (for RD179-1 using TPD4164F).

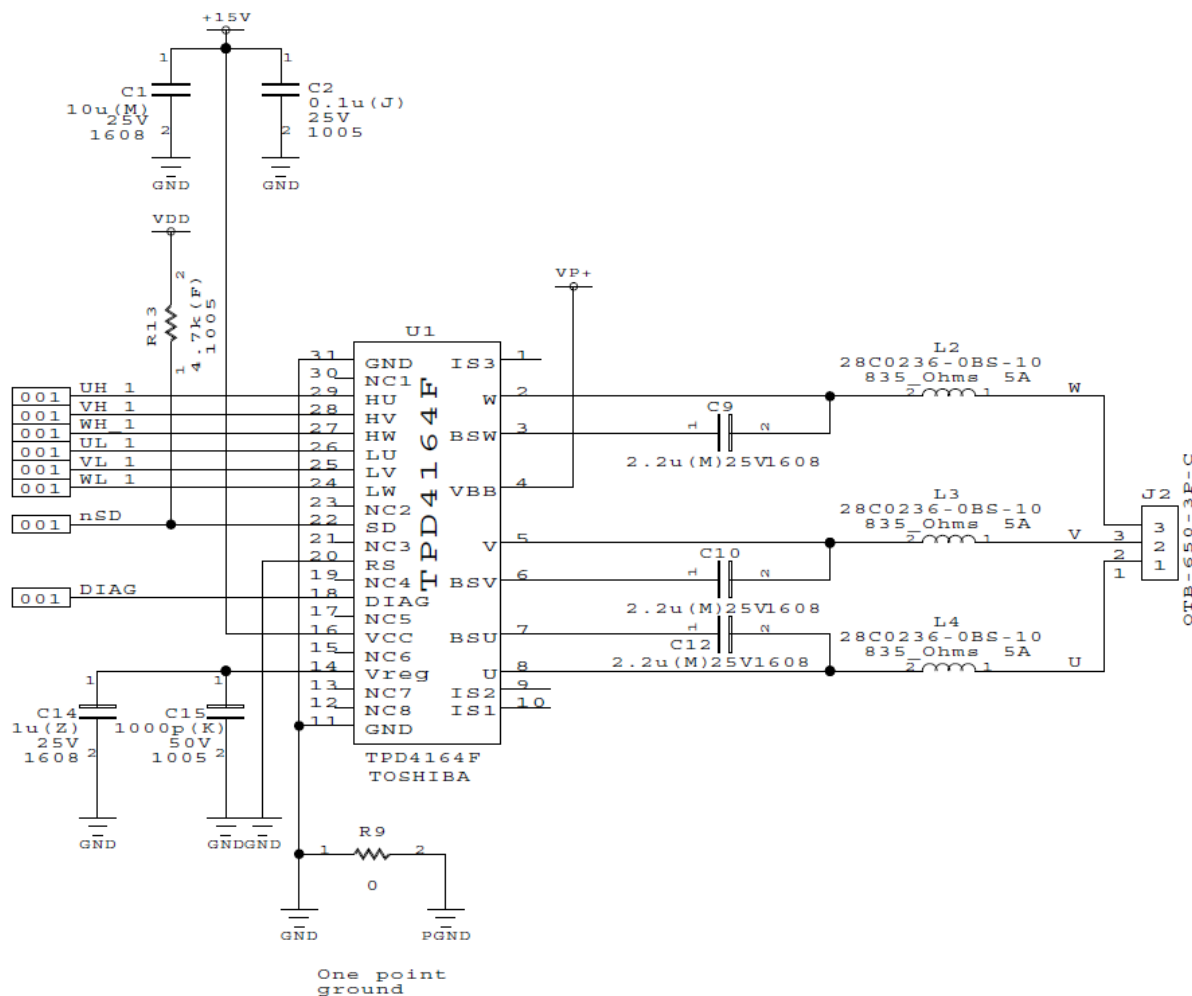


Fig. 3.3 Motor Drive Circuit (For RD179-1 using TPD4164F)

The intelligent power device (U1, TPD4164F in RD179-1) has built-in gate driver, and the 5 V level inverter control signals (UH_1, VH_1, WH_1, UL_1, VL_1, WL_1) output from the MCU can be directly connected to the HU pin, HV pin, HW pin, LU pin, LV pin, and LW pin. The inverter output from the U, V, and W pins are output to the motor connection terminals (J2) via filters (L2, L3, and L4).

The motor power (VP+) is supplied from the motor power input terminal (J1) to V_{BB} pins. The motor power ground (PGND) is connected to the control power ground (GND) at a single point. The 15 V control power is supplied from the control power input terminal (J3) to V_{CC} pin. A power supply stabilizing capacitor (C1) and a surge absorbing capacitor (C2) are connected to the control power supply.

The intelligent power device has a built-in bootstrap diode required for level shifting of the high-side gate driver. Connect a bootstrap capacitor (C9, C10, C12, 2.2 μ F 25 V each) between U-pin and BSU-pin, between V-pin and BSV pin, and between W-pin and BSW pin.

The U1 has a built-in regulator and can output 5 V (for RD179-1) to V_{REG} pin, but it is not used in this reference design. Regardless of the use of the internal regulator output, connect a power supply stabilizing capacitor (C14) and a surge absorbing capacitor (C15) to V_{REG} pin of U1.

The SD pin of U1 is the shutdown control signal input. When the L level is input, all inverter outputs are shut off. This reference is connected to the MCU and is pulled up to VDD (5 V) by R13.

The input-side control pin and output-side step-down large current pin of the U1 are separated on both sides of the package. However, it is necessary to consider the creepage distances, etc., while designing the pattern.

3.3. Shunt Current Measurement Circuit

Fig. 3.4 shows the shunt current measurement circuit (for RD179-1 using TPD4164F).

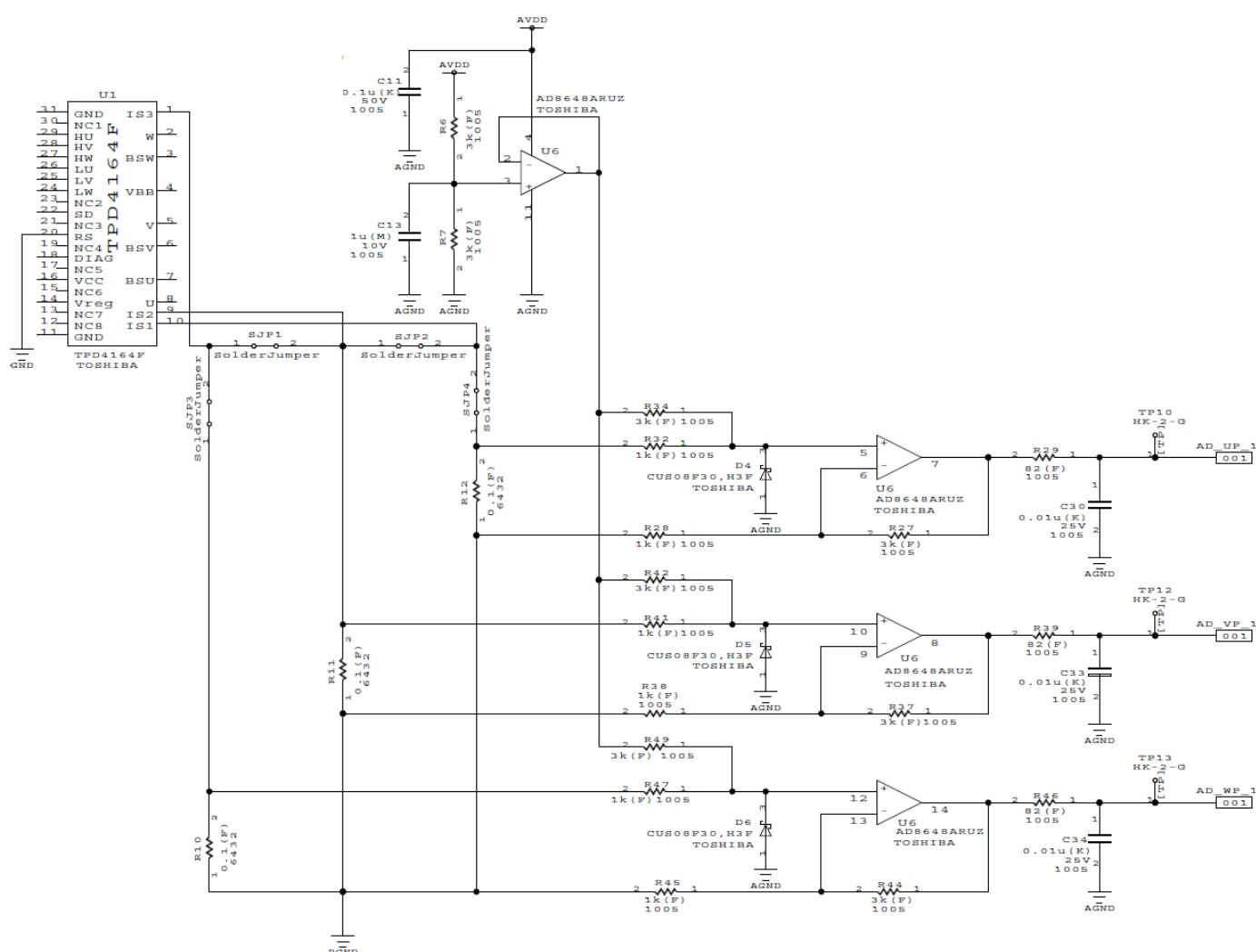


Fig. 3.4 Shunt Current Measurement Circuit (for RD179-1 using TPD4164F)

Intelligent power devices have shunt resistor connection pins for each half-bridge of the output inverter. IS1 pin corresponds to the U-phase output bridge, IS2 pin corresponds to the V-phase output bridge, and IS3 pin corresponds to the W-phase output bridge. In this design, a shunt

resistor (R12, R11, R10, 0.1 Ω respectively) is connected to each pin, and amplified with 3 times gain by the operational amplifier (U6).

Bias voltage is added so that the output voltage becomes 2.5 V when the shunt current is 0 A. The op-amp with pin 1, pin 2, and pin 3 of U6 operates as a voltage follower of 2.5 V generated by the voltage divider circuit made of R6 and R7, and provides a bias voltage to the op-amps of each phase.

The shunt current measurement signals (AD_UP_1, AD_VP_1, AD_WP_1) are input to the A/D converter of the MCU via RC LPF (R29 and C30, R39 and C33, R46 and C34). The cutoff frequency f_c of this LPF is as follows.

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 82 \times 0.01 \times 10^{-6}} \approx 200 \text{ kHz}$$

The three-shunt configuration and one-shunt configuration can be changed in this reference design. Three-shunt configuration is selected by opening the solder jumper SJP1 and SJP2, shorting SJP3 and SJP4, and one-shunt configuration is selected by shorting the solder jumper SJP1 and SJP2, and opening SJP3 and SJP4. Only the V-phase shunt current measurement signal (AD_VP_1) is used in the 1-shunt configuration.

3.4. Error Detection Circuit

Fig. 3.5 shows the error detection circuit.

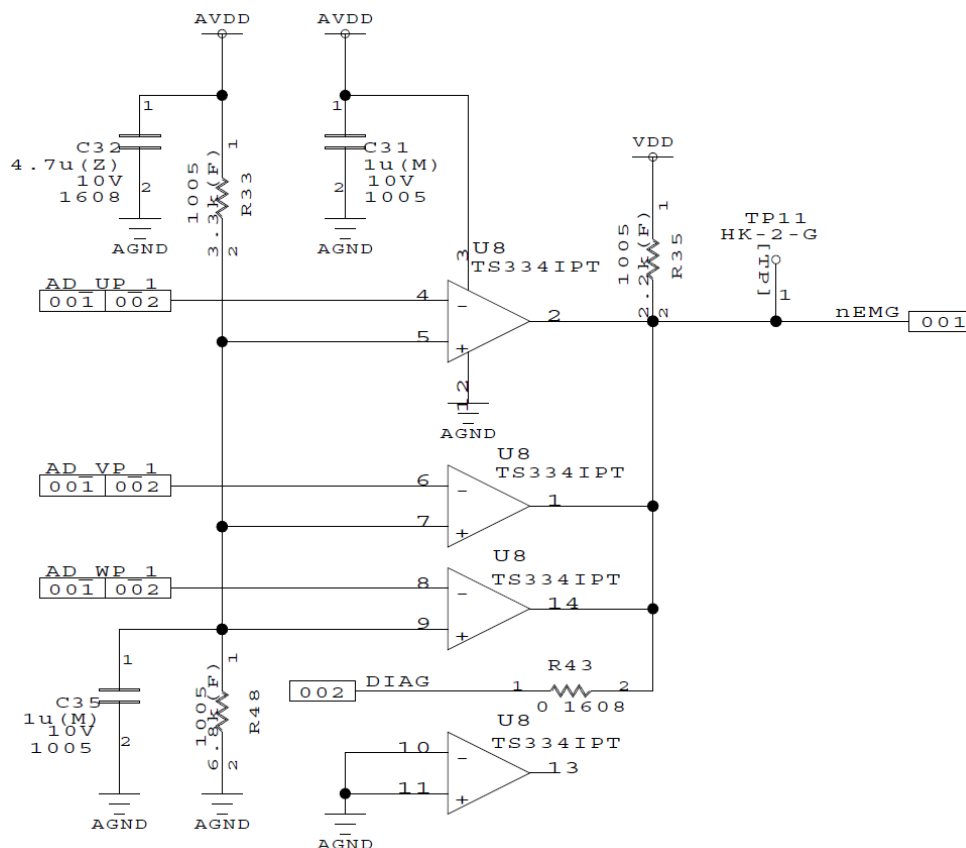


Fig. 3.5 Error Detection Circuit

The shunt current measurement signals (AD_UP_1, AD_VP_1, AD_WP_1) of each phase are used to detect an overcurrent error by using the comparator (U8). Since the overcurrent error output of each phase from the comparator and the diagnostic output (DIAG) signal of the intelligent power device (U1) are either open collector or open drain output, a wired OR output is generated by using the pull-up resistor (R35), and the resulting error detection signal (nEMG) is connected to the EMG pin of the MCU. Whenever an error occurs in either one of them, nEMG signal is sent to the EMG pin of the MCU.

The + side reference voltage (approx. 3.37 V) of the comparator is produced by dividing AVDD (5 V) using R48 and R33. When the shunt current of each phase is i , the shunt current measurement voltage v input to each comparator is

$$v = 2.5 + i \times 0.1 \times \text{OpAmpGain}(3.0)$$

Therefore, when the shunt current of each phase becomes about 2.89 A or more, an error detection signal is output.

3.5. Motor Voltage Detection Circuit

Fig. 3.6 shows the motor voltage detection circuit.

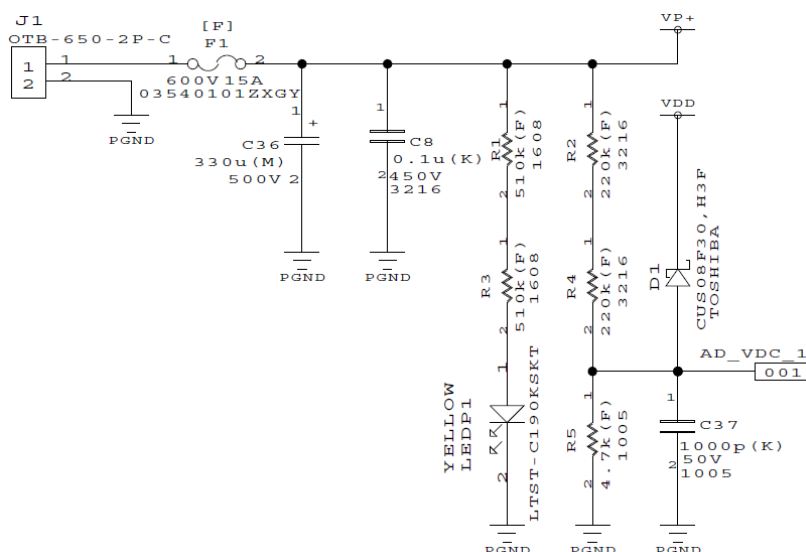


Fig. 3.6 Motor Voltage Detection Circuit

The motor voltage (VP +1) input from the motor power terminal (J1) is divided by the resistors (R2, R4, R5) and is input to the A/D converter of the MCU as the motor voltage signal (AD_VDC_1). The motor voltage signal input to the A/D converter is approximately $0.01 \times (VP+)$, i.e. approximately 1 % of the motor voltage.

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