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Investigation of the Breakdown Voltage Degradation under Hot-Carrier Injection in STI-based PchLDMOS Transistors

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***Abstract*—Hot-carrier injection causes characteristics change of semiconductor devices. In this work, off-state breakdown voltage (BVdss) degradation of shallow trench isolation (STI) based PchLDMOS under drain avalanche hot-carrier (DAHC) stress has been investigated. We found that the cause of the degradation was a trapped charge at the bottom area of STI rather than STI corner. The mechanism of BVdss degradation was clarified and a tolerant LDMOS structure is proposed.**

Keywords— PchLDMOS; Hot-carrier; Reliability; BVdss degradation

I. INTRODUCTION

Shallow trench isolation (STI) has been commonly used for LDMOS transistors in mixed-signal ICs, which include low-voltage CMOS devices for logic circuits and high-voltage LDMOS devices for analog circuits. STI, which is used for device isolation, can be applied to LDMOS in order to suppress the electric field between its source and drain and thus be able to scale down the device dimensions [1]. However, it is known that the STI structure also causes and enhances hot-carrier induced degradation [2]. As for the hot-carrier induced PchLDMOS characteristics degradation, the gate oxide breakdown has been widely reported [3]. On the other hand, few papers reported off-state breakdown voltage (BVdss) degradation under drain avalanche hot-carrier (DAHC) stress, which is also a critical issue for high voltage LDMOS devices. Thus far, it is considered that this BVdss degradation occurs due to trapped charge around the corner of STI, where the impact-ionization rate is the highest [4]. It is important to understand this phenomenon more deeply to design the high reliable devices. In this paper, the BVdss degradation of PchLDMOSs was intensively studied by device measurement and TCAD simulation in two types of structures: a structure that has p type drift region surrounded by a p- region (DRIFT) and a reduced surface field (RESURF) structure. As a result, we reached a conclusion that the cause of the degradation is trapped charge at the STI bottom rather than STI corner.

II. DRIFT PCHLDMOS STRUCTURE

A. Device structure and Measurements

Cross sectional view of the DRIFT PchLDMOS with 0.13 µm CMOS-DMOS technology is shown in Fig. 1(a). In order to determine the DAHC stress condition, Ig - Vgs curve was measured (Fig. 1(b)). The Vgs at the Ig_max is used as the condition of DAHC stress which the impact-ionization occurs the most. Fig. 1(c) shows the breakdown characteristics of a 40V DRIFT PchLDMOS under the DAHC stress, and it is shown that the BVdss decreases immediately after the test started and decreases continuously during the test (Fig. 1(d)).

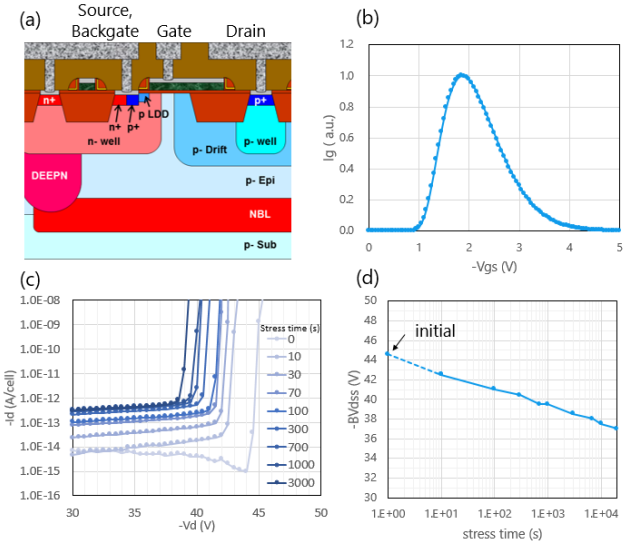

Fig. 1: (a) Cross-sectional view of the DRIFT PchLDMOS structure, (b) Measured Ig-Vgs curve of the PchLDMOS (Vds = -40V, -40°C), (c) Measured breakdown characteristics of the PchLDMOS under DAHC stress (stress condition: Vds = -40V, Vgs = -1.85V, -40°C) and (d) Dependence of BVdss (Ids = -0.01 µA/cell) on DAHC stress time (stress condition: Vds = -40V, Vgs = -1.85V, -40°C).

B. Simulation results and BVdss degradation mechanism

Fig. 2 shows the TCAD (Synopsys Sentaurus) simulated results of the PchLDMOS under the DAHC stress. A peak of impact-ionization exists at the STI corner (Fig. 2(a)). However, it is noted that the strong vertical electron attractive electric field (*ElectricField-Y*) exists at the bottom of STI (Fig. 2(b)). The amount of *ElectricField-Y* has two peaks both at the STI corner and STI bottom. In the case of the STI corner, the horizontal electron attractive electric field (*ElectricField-X*) is larger than the *ElectricField-Y*, and it results in hot-electron flowing to the source direction without being injected into the STI corner. On the contrary, the *ElectricField-Y* at the STI bottom is larger and dominates the hot-electron flow, which results in injection into STI bottom region. Therefore, it is considered that the hot-electron is injected and trapped at the STI bottom region rather

than STI corner. Fig. 3 is the distribution of trapped negative charge after 1 x 10^5 s of DAHC stress calculated by TCAD simulation. It is shown that the trapped negative charge distributed along STI/Si interface, and has a peak at the STI bottom some distance away from the STI corner. To estimate the influence of trapped negative charge on BVdss, BVdss of the PchLDMOS with fixed negative charge at the bottom of the STI is simulated (Fig. 4). It is verified that the BVdss decreases due to the fixed negative charge at the STI bottom, even though no fixed negative charge is added at the corner of STI.

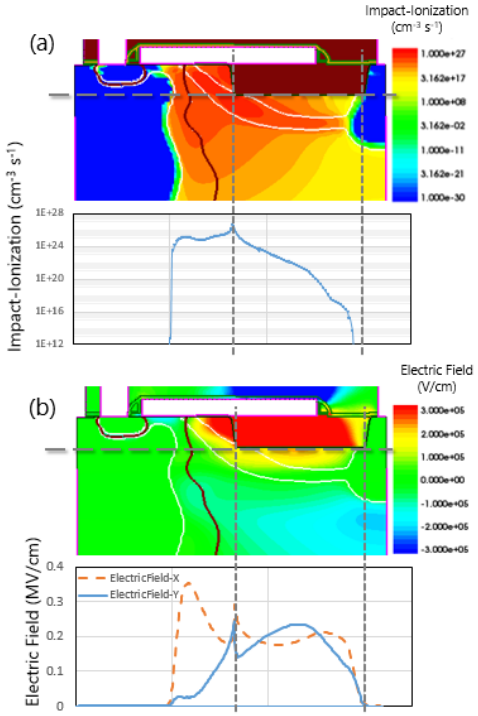

Fig. 2: 2D TCAD simulation results and 1D horizontal profiles under the STI bottom region: (a) Impact-ionization and (b) Electric field distribution during DAHC stress (Vds = -40V, Vgs = -2.0V, 27°C).

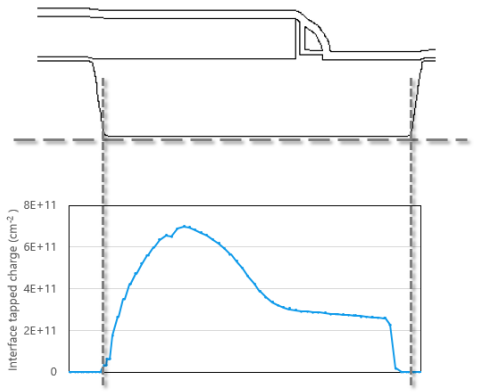

Fig. 3: 1D horizontal profile of trapped negative charge at the interface between STI bottom and Si after 1×10^5 s of DAHC stress (Vds = -40V, Vgs = -2.0V, 27°C).

To understand this phenomenon further, electric field distribution at BVdss measurement condition (Vds = -40V, Vgs = 0V) with fixed negative charge along the STI bottom is simulated (Fig. 5). As the amount of fixed negative charge increases, electric field of the STI bottom (point (iii)) decreases, while the other points (i), (ii) and (iv) increase. Therefore, the breakdown voltage is degraded because of the collapse in the balance of the electric field distribution in the drift region. This electric field change can be explained as follows. The trapped electron at the STI/Si interface attracts hole, which lowers the resistance beneath the STI bottom. As a result, electric field at the bottom of the STI decreases (Fig. 5(d) and Fig. 6), and electric field at the STI corner is intensified instead.

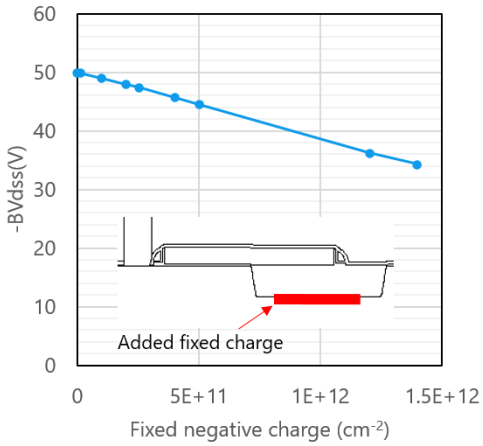

Fig. 4: Simulated BVdss dependence of the DRIFT structure on fixed negative charge at the STI bottom.

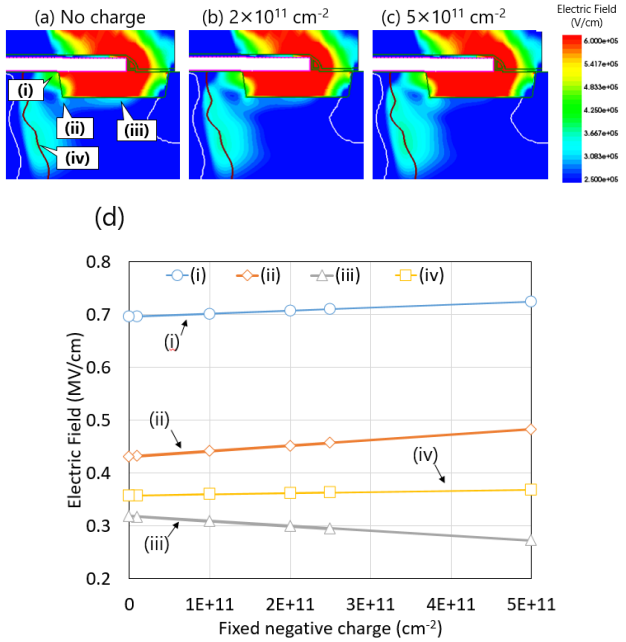

Fig. 5: Electric field distribution of the DRIFT PchLDMOS (Vds = -40V, Vgs = 0V, 27°C) with fixed negative charge at the STI bottom: (a) No charge, (b) 2×10^{11} cm^{-2} , (c) 5×10^{11} cm^{-2} and (d) The maximum intensity of electric field at each region.

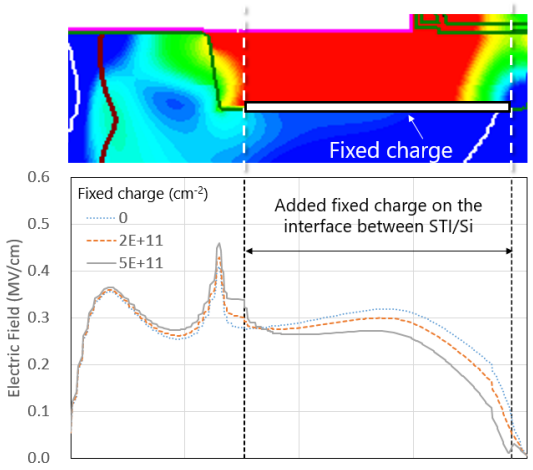

Fig. 6: Dependence of the electric field of the DRIFT PchLDMOS (Vds = -40V, Vgs = 0V, 27°C) on the fixed negative charge.

III. RESURF PCHLDMOS STRUCTURE

A. Device structure and Measurements

As a result of the DRIFT PchLDMOS structure, the RESURF PchLDMOS structure (Fig. 7(a)) could be a candidate which is tolerant against the BVdss degradation. The existence of an additional junction underneath the drift region would be expected to share the total electric field of drift region. Fig. 7(b) shows dependence of BVdss of a 40V RESURF PchLDMOS on DAHC stress time, with the result of the DRIFT structure case. As for the RESURF structure, the BVdss degradation does not occur until 1×10^3 s, and it is clearly more tolerant against BVdss degradation than DRIFT structure.

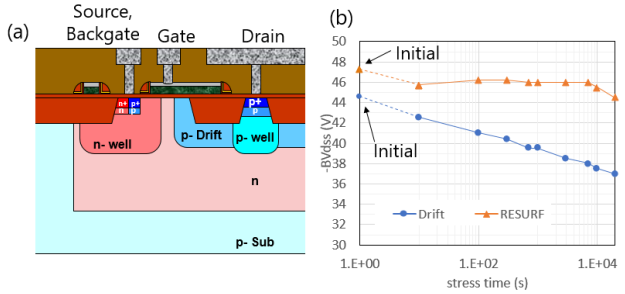

Fig. 7: (a) Cross-sectional view of the RESURF PchLDMOS structure. (b) Measured breakdown characteristics of the RESURF PchLDMOS under DAHC stress (stress condition: Vds = -40V, Vgs = -1.90V, -40°C) and the DRIFT PchLDMOS.

B. Simulation results and BVdss degradation mechanisms

Same TCAD simulations as the DRIFT structure were carried out (Fig. 8). These results confirmed that, also in the case of the RESURF structure, the distribution of the *ElectricField-X, Y,* and hot-electron induced trapped negative charge position show similar tendency to DRIFT structure. BVdss dependence of the RESURF structure on fixed negative charge was also simulated (Fig. 9). As already observed in the DRIFT structure, the fixed negative charge at the STI bottom decreases its BVdss (Fig. 4), however, as for the RESURF structure, it is noted that the BVdss improved by adding trapped negative charge up to

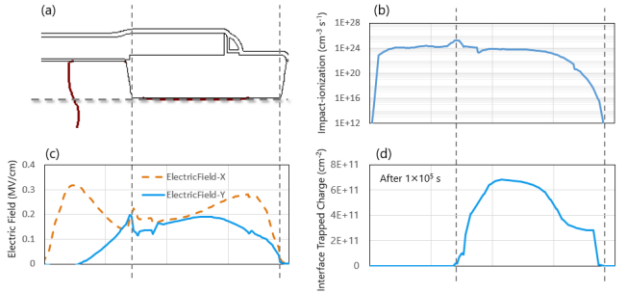

Fig. 8: (a) Cross-sectional view of the RESURF PchLDMOS. 1D profiles under the STI bottom of the PchLDMOS: (b) Impact-ionization and (c) Electric field at DAHC stress (Vds = -40V, Vgs = -2.0V, 27°C), and (d) Interface trapped negative charge after 1×10^5 s of the DAHC stress.

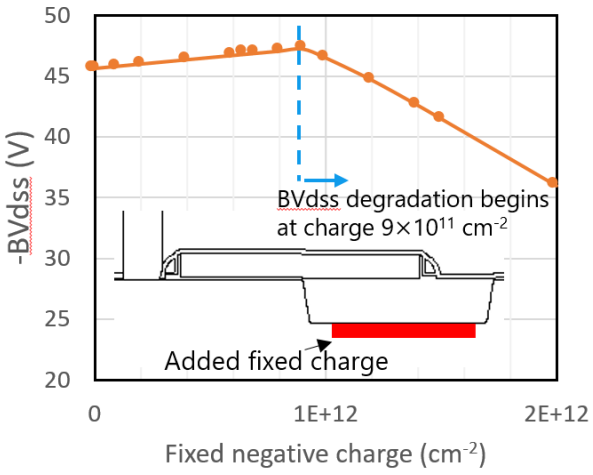

Fig. 9: Simulated BVdss dependence of the RESURF structure on fixed negative charge at the STI bottom.

9×10^{11} cm^{-2}, and after the trapped negative charge exceed a threshold amount, the BVdss starts decreasing. This result has a good agreement with the measurement result (Fig. 7(b)).

Electric field distribution of the RESURF structure under BVdss condition (Vds = -40V, Vgs = 0V) with fixed negative charge along STI bottom was also simulated (Fig. 10). In the case of the RESURF structure, a higher electric field at the bottom of drain (point (v)) is added compared to the DRIFT structure. As the trapped negative charge increases, the electric field intensity at point (iii) and (v) decrease, while the other points (i), (ii) and (iv) increase. When the trapped negative charge is larger than 8×10^{11} cm^{-2}, the electric field intensity at point (ii) exceeds that at point (v). This result corresponds to the relation between the BVdss degradation and the electric field distribution balance. In order to investigate this breakdown behavior at the conversion point, further TCAD simulation was carried out. Fig. 11 shows the electron and hole current density distributions at the fixed negative charge of 8×10^{11} and 1×10^{12} cm^{-2}, which show the states before and after the electric field intensities at point (v) and (ii) are reversed. When the electric field of point (v) is higher than (ii), electron flows through the point (v) (Fig. 11(a)). Due to this current, potential of the n-type region under the drift region is negatively biased and a parasitic p-n-p transistor, which consists of the emitter (source), the base

(backagate) and the collector (drain), is turned on. This parasitic p-n-p transistor current causes the drain-source breakdown. Whereas, after the electric field intensity at the point (ii) exceeds the point (v), the hole current flows from the source to drain via the STI corner (Fig. 11(d)), which suggests that the breakdown occurs at the STI corner. These results can explain the different BVdss degradation behavior of the RESURF structure from DRIFT structure. The existence of point (v), which is the region insusceptible to STI trapped negative charge, suppresses BVdss degradation to the extent that the electric field at point (ii) is less than that of point (v). After the electric field at point (ii) exceeds that at point (v), the BVdss degradation starts by the same mechanism as the DRIFT structure, which is caused by the collapse of electric field distribution balance in the drift region. Therefore, the RESURF structure is tolerant against the BVdss degradation.

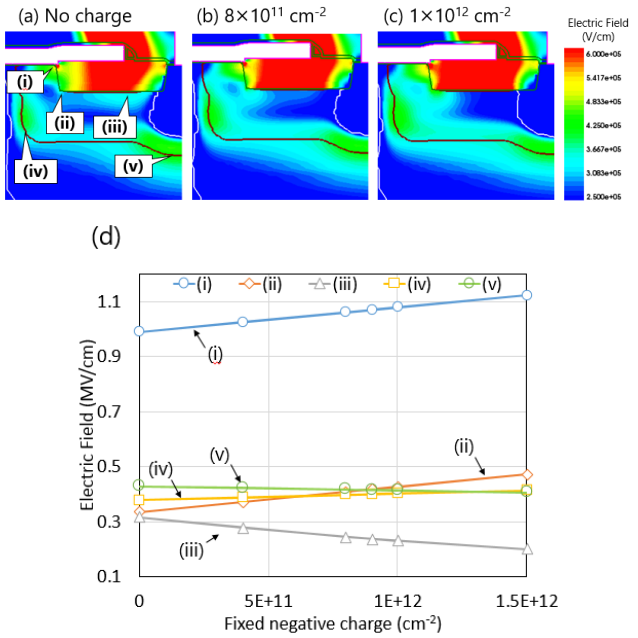

Fig. 10: Electric field distribution of the RESURF PchLDMOS (Vds = -40V, Vgs = 0V, 27°C) with fixed negative charge at the STI bottom: (a) No charge, (b) 8×10^{11} cm^{-2}, (b) 1×10^{12} cm^{-2} and (d) The maximum intensity of electric field intensity at each region.

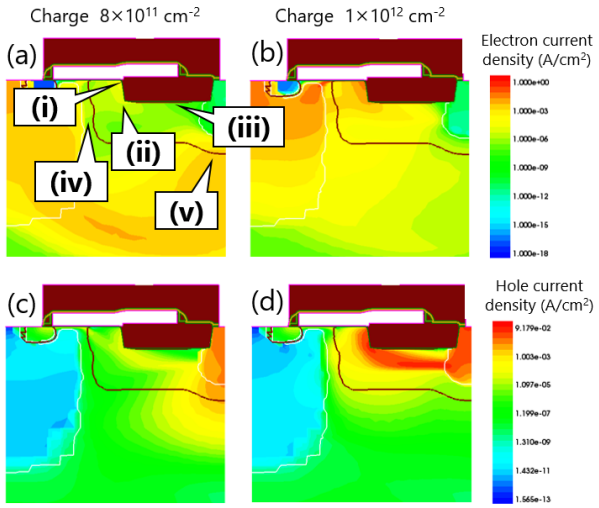

Fig. 11: The distributions of electron and hole current density at the breakdown of the RESURF PchLDMOS (Vds = BVdss, Vgs = 0V, 27°C) with fixed negative charge: (a) Electron current density at fixed negative charge 8×10^{11} cm^{-2} and (b) 1×10^{12} cm^{-2} ; (c) Hole current density at negative charge 8×10^{11} cm^{-2} and (d) 1×10^{12} cm^{-2}.

IV. Conclusion

In this work, BVdss degradation of STI based PchLDMOS under the DAHC stress has been investigated for both DRIFT and RESURF structure. We found that the cause of the degradation was the trapped negative charge at STI bottom rather than STI corner. We also clarified the mechanisms of the breakdown behavior, which is different between DRIFT and RESURF structures. RESURF structure realizes high tolerance against BVdss degradation due to the existence of an additional junction beneath the drain region.

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