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Design Method and Mechanism Study of LDMOS to Conquer Stress Induced Degradation of Leakage Current and HTRB Reliability

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***Abstract*—8V NchLDMOS, which has an enough tolerance against both a leakage current (Idss) increase and high temperature reverse bias (HTRB) degradation is proposed. Dislocation growth, which results in Idss increase and has a negative influence on HTRB reliability, occurs because of a high-dose ion implantation and/or mechanical stress due to shallow trench isolation (STI). The studied 8V NchLDMOS was developed by taking into account the mechanism understanding to prevent the dislocation growth affecting the device characteristics, and as a result, achieved a competitive low resistance (RonA=1.67mΩ.mm^2).**

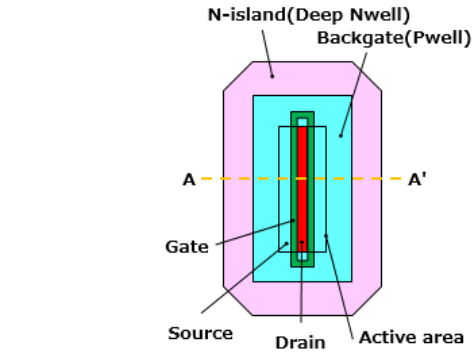
Keywords—LDMOS, dislocation growth, leakage current, high temperature reverse bias

I. Introduction

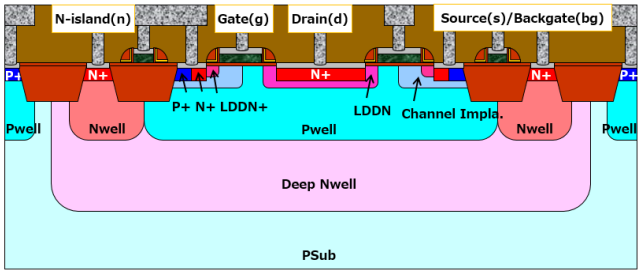
LDMOS is widely used for Mixed-signal ICs. In case of using for output devices, LDMOS's size, which has a considerable impact on the total chip size, is an important factor. Therefore, low on-resistance (Ron) is an indispensable characteristics of LDMOS [1-5]. At the same time, keeping the LDMOS's Idss low is also significant in order to realize a low stand-by power. Moreover, Idss increase during the product operation leads to circuit operation failure and IC's lifetime degradation. A number of studies have been done to design a low-Idss device [6] with obtaining a high yield [7] and also to suppress Idss increase from the reliability viewpoint [8-9]. In this study, we focus on the relation between device characteristics and the impact of the mechanical stress due to STI, and propose the device design which is tolerate against both Idss increase and high HTRB degradation with keeping a low Ron.

II. Device Structures and Experiment

The device was fabricated using 0.13 µm CMOS-DMOS technology [8]. Plane and cross-sectional schematic views of conventional 8V NchLDMOS are shown in Fig.1. In the evaluated device, the channel length is 0.3 µm and the gate oxide thickness is 12.5 nm. The off-state drain-source breakdown voltage (BVdss) is 10 V, which can ensure 8 V operation considering BVdss variance and temperature dependence. The source and the backgate electrodes were shorted by layout design. STI is located only at the outer region of the device. In this study, two kinds of STI filling materials were studied, since STI filling material remains in the device structure, that it has a great influence on the device characteristics, yield, and reliability. Material-A is deposited by a method of a high density plasma assisted chemical vapor deposition (CVD) processing and material-B is deposited by an atmospheric pressure CVD processing.



(a)



(b)

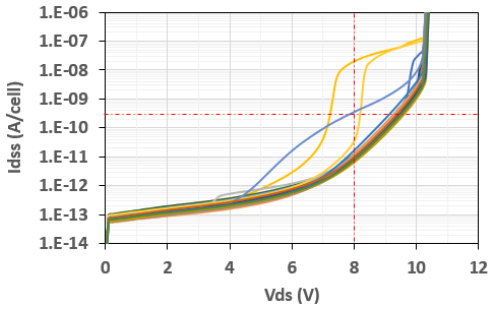
Fig. 1: (a) Plane and (b) cross-sectional views (A-A') of a conventional 8V NchLDMOS structure.

III. Results and Discussions

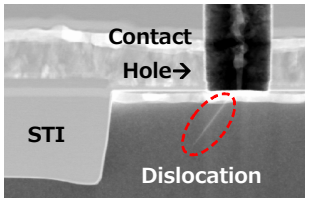
A. Initial leakage current

Id-Vd curves of the conventional structure which applied material-A as a STI filling material (Fig. 2(a)) show that some of the chips have Idss which excesses 3pA/cell below Vds=8V. Fig. 2(b) is a TEM image of the fail chip. The dislocation was observed under the contact hole near the STI. A high-dose ion implantation forms an amorphous Si layer. The annealing follows to activate the amorphous Si layer, and during a recrystallization, the Si is activated under the

high stress due to the STI filling material, which has a different thermal expansion coefficient compared to Si. While the recrystallization carries on, the value of STI induced stress which affects the Si might excess a critical stress, which results in the dislocation formation. We assume that the origin of the dislocation might be the high-dose ion implantation damage combined with STI stress, and thus, we investigated an influence of high-dose ion implantation damage on the Idss failure rate and the Ron (Fig. 3). As the phosphorus dose decreases, the defect generation decreases. However, decreasing the phosphorus dose results in the Ron increase simultaneously, thus this approach is not preferable for LDMOS performance. Although applying a thermal process for a long time to recover the Si damage caused by high-dose ion-implantation is not suitable for a shrunk process because of a design restriction. Meanwhile, we also studied two kinds of STI filling material having different stress against Si, material-A shows higher stress during annealing than material-B, and stress value are dependent on their film density. In the case of applying the material-B, no Idss fail chip was observed even at $4.6x10^{15}$ cm^{-2} dose condition (Fig. 4), although some fail chips were observed at the same dose condition in the case of material-A (Fig. 2(a)).



(a)



(b)

Fig. 2: (a) Idss-Vds curves (Vgs=0V, T=27ºC) of conventional structure with STI filling material-A at $4.6x10^{15}$ cm^{-2} dose condition (b) cross-sectional TEM image of the fail chip.

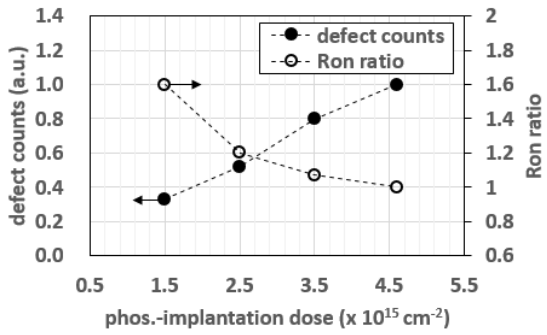


Fig. 3: Dependence of the *Idss failure rate and the Ron of conventional structure with STI filling material-A on Phos. dose. *3200cell array pattern of 8V NchLDMOS

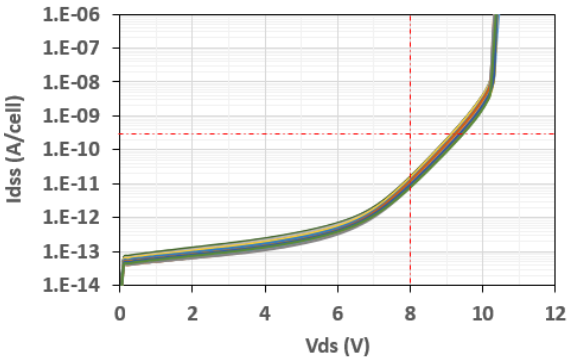
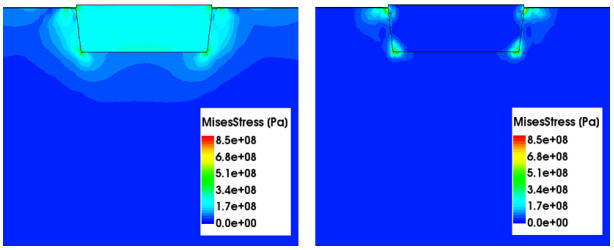


Fig. 4: Idss-Vds curves (Vgs=0V, T=27ºC) of conventional structure with STI filling material-B at $4.6x10^{15}$ cm^{-2} dose condition.



(a) (b)

Fig. 5: Simulation results of Mises stress applying (a) material-A and (b) material-B as a STI filling material. Applied stress is -300MPa and 0MPa, respectively.

To evaluate the stress difference between material-A and B, a process simulation was carried out based on the estimated stress value, -300MPa in material-A and 0Mpa in material-B, respectively. These values were calculated from the warp evaluation on bare wafers [9]. Fig. 5 shows a calculated stress distribution during the densification under the high temperature annealing which has a strong relation to the dislocation growth. In the case of material-A, higher stress value is observed at the Si substrate near a STI, and it is suppressed in material-B case. This high stress prevents the recrystallization of the Si, thus leaves the dislocation. The simulated results well describe the Idss-Vds characteristics difference between material-A and B (Fig. 2(a) and Fig. 4).

B. High temperature reverse bias (HTRB)

We assume that this Idss failure rate difference occurs from dislocation growth rate related to Si stress from STI filling materials. HTRB test was also carried out to evaluate the influence of STI stress. The Idss continuously increased under the HTRB stress for both material-A and B (Fig. 6). The results indicate that reducing the stress from the STI filling material is not enough to ensure the reliability. Further approach is needed to prevent the Idss increase under the HTRB stress. The HTRB degradation could be caused by the trapped charge at STI/Si-interface [10], in that case, the trapped charge is de-trapped by applying wafer baking after HTRB test, which leads to Idss increase suppression. However, the result of wafer baking showed Idss increase (Fig. 7). The result is unreasonable with the assumption, and thus we propose another mechanism to explain this phenomenon.

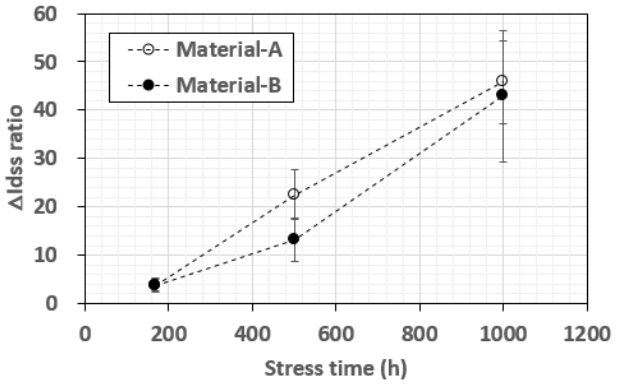


Fig. 6: Measured Idss/Idss0 (Vds=8V, Vgs=0V, T=27ºC, 8 points) under the HTRB stress (Vds=8V, Vgs=0V, T=150ºC) of conventional structure with STI filling material-A and B.

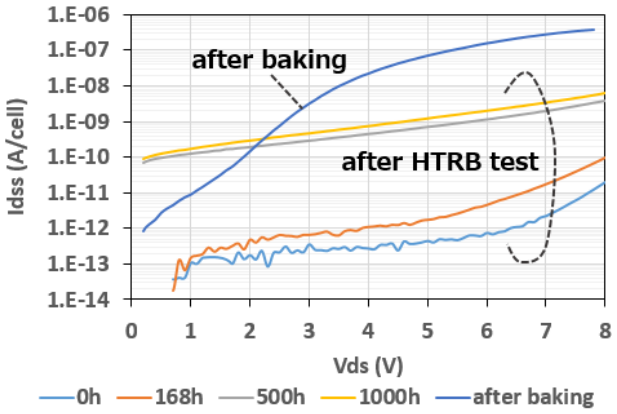


Fig. 7: Measured Idss-Vds (Vgs=0V, T=27ºC) of conventional structure with STI filling material-A under the HTRB stress (Vds=8V, Vgs=0V, T=150ºC) and after wafer baking for 24h at 250ºC.

IV. Mechanism of Idss Increase Under the HTRB Stress

Fig. 8 shows the explanation of the mechanism of Idss increase under the HTRB stress. Idss increase after HTRB is considered to relate to both H+ termination to a dislocation and de-termination from the dislocation. Firstly, the dislocation due to high-dose implantation near the STI/Si edge grows. Secondly, the dislocation is treated by hydrogen (H+) termination to the dangling bond under the N_2/H_2 anneal. This is because the Idss at 0s show low Idss (Fig.7). In spite of this H+ termination during N_2/H_2 anneal, H+ de-terminates from the dangling bond under the HTRB stress. As a result, the leakage current after the HTRB stress increases. From this assumption, the cause of the Idss increase under the HTRB stress is as same as the Idss failure rate increase due to a dislocation growth. In order to prevent the dislocation growth, the first approach is to select a preferable STI filling material, which to suppress a stress inside the Si less than its critical stress. However, just modifying the STI filling material was not enough to prevent HTRB degradation (Fig.6). Additional approach is needed, that is to suppress the value of the critical stress of the specific area inside the Si near the STI, where the high stress exists. In particular, the high-dose implanted area should be kept away from the highly stressed area close to the STI by modifying the LDMOS layout design. Fig. 9 shows plane and cross-sectional schematic views of (a) conventional and (b) GC-covered structure, which STI/Si-interface is covered by gate poly Si. Modified structure (Fig. 9(b) and (d)) keeps high-dose ion implantation area away from STI/Si-interface. The HTRB result of GC-covered structure with STI filling material-B is shown in Fig. 10. In comparison to the HTRB result of the conventional structure (Fig. 6), in spite of the stress condition is severe for the GC-covered structure, which the HTRB test of conventional structure took place under 150ºC/1000h, while new structure was 175 ºC/2000h, the ratio of Idss compared to initial Idss (Idss/Idss0) was 45 and <1. These results demonstrate that the solution came out from the HTRB degradation mechanism (Fig.8), which to keep the high-dose implanted area away from the STI was meaningful to suppress Idss increase under the HTRB stress. In conclusion, it is necessary to take into account the high dose ion implantation damage as well as STI's mechanical stress due to STI filling material's density at the same time. As a result, competitive low resistance (RonA =1.67mΩ.mm^2) LDMOS has been successfully fabricated (Fig. 11).

Mechanism of leakage current increase under HTRB stress

(1) Growth of the dislocation due to high-dose implantation near the STI/Si edge
(2) Treatment of the dislocation by hydrogen (H+) termination to the dangling bonds under the N_2/H_2 anneal
(3) H+ de-termination from dangling bonds under the HTRB
(4) Increase of the leakage current after HTRB stress

*Wafer baking after HTRB accelerates the H+ de-termination and increases the leakage current

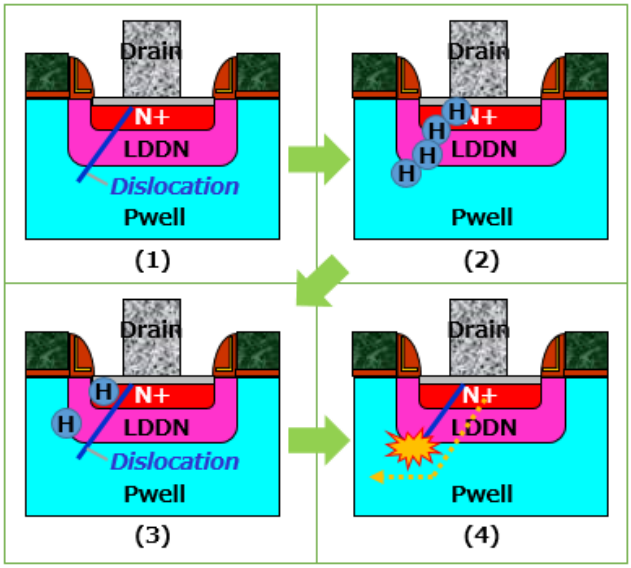


Fig. 8: Explanation of the mechanism of leakage current increase under the HTRB stress.

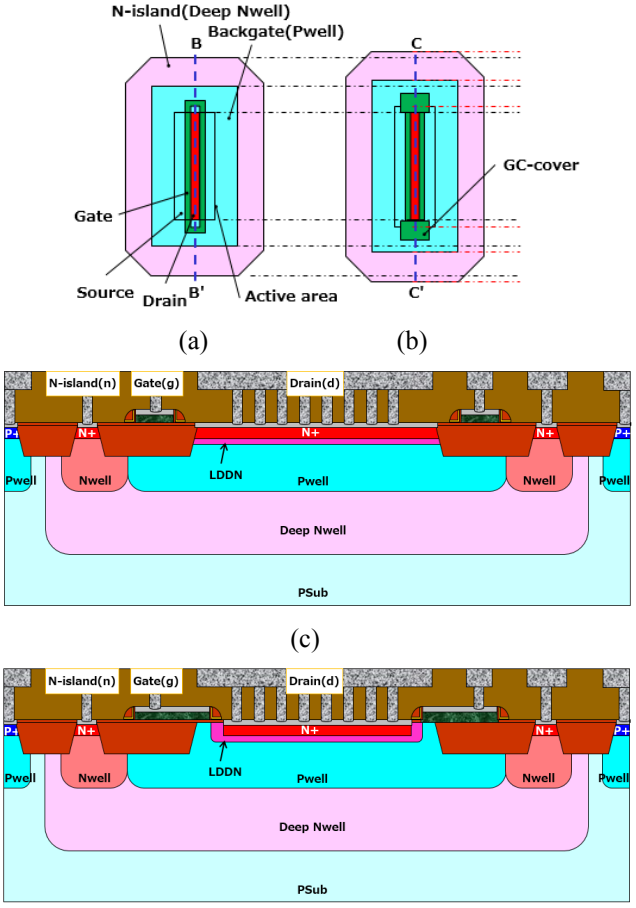


Fig. 9: Plane and cross-sectional views of (a) and (c) conventional and (b) and (d) GC -covered structure.

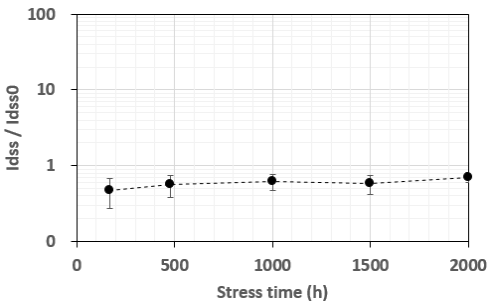


Fig. 10: Measured Idss/Idss0 (Vds=8V, Vgs=0V, T=27ºC, 8 points) under the HTRB stress (Vds=8V, Vgs=0V, T=175ºC) of GC-covered structure with STI filling material-B.

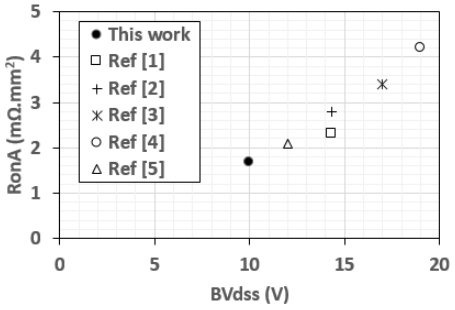


Fig. 11: Comparison of the RonA vs. BVdss for NchLDMOS.

V. Conclusions

8V NchLDMOS, which has a tolerance against a leakage current (Idss) increase and high temperature reverse bias (HTRB) degradation is proposed. Dislocation growth, which results in Idss increase and has a negative influence on HTRB reliability, occurs because of a high-dose ion implantation and/or mechanical stress due to shallow trench isolation (STI). The studied 8V NchLDMOS was developed by taking into account the mechanism understanding, which to prevent the dislocation growth affecting the device characteristics. As a result, both enough tolerance against HTRB stress and low leakage current with a competitive low resistance (RonA=1.67mΩ.mm2) has been achieved.

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