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Paralleling 3.3-kV/800-A rated SiC-MOSFET Modules: An Optimization Method

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Abstract

When power semiconductor modules are connected in parallel, the switching characteristics and current imbalance of each device need to be aligned. This paper focuses on the mutual inductance between the gate driver and the main circuit and the stray inductance of the main circuit when a silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) module with a rating of 3.3 kV/800 A is operated in parallel, to examine the effect on the switching operation and describe the optimum method. First, the effect of mutual inductance between the gate wiring of devices in parallel and the main circuit was evaluated by performing actual measurements, and it was shown that gate voltage fluctuations could be suppressed by bringing the gate wiring of each device closer together. Next, when an external capacitor C_{gs} was inserted as a gate-noise countermeasure, it was shown that reducing the loop between the main circuit and the capacitor could decrease the mutual inductance and lessen the difference in switching characteristics. Finally, the difference in stray inductance of the main circuit of each device was evaluated. Differences in stray inductance of the main circuit cause current imbalance, resulting in differences in the loss of each device. As a result, there is a difference in the thermal fatigue life of each device, and the expected life of the system is shorter than anticipated. It is therefore important to match stray inductances of the main circuits within the range where turn-off surges are allowed.

1 Introduction

In inverters with capacities exceeding several hundred kilowatts, such as those used in the rail, industrial, and energy sectors, it is common practice to connect them in parallel when it is difficult for a single power semiconductor module to meet the capacity of the equipment [1] [2]. When power semiconductor modules are connected in parallel, the current imbalance needs to be reduced, and the switching characteristics need to be matched in order to ensure uniform electrical and thermal stress and to prevent malfunctions due to resonance between modules [3] [4]. This section describes the general issues to be considered in parallel drives using metal-oxide-semiconductor-field effect transistors (MOSFETs) in terms of devices, gate drivers, and main circuits.

First, it is important to match the characteristics of the devices constituting the parallel circuit as closely as possible. In particular, deviations in the MOSFET threshold voltage V_{th} lead to resonance and other problems due to timing deviations during switching, while on-resistance generates current imbalance [5].

Next, there are two methods for connecting gate drivers: one in which each device connected in parallel is driven by an individual gate driver, and the other in which a common gate driver is used. When using individual gate drivers, the gate-drive circuits for each device are separated, thereby reducing the risk of malfunctions due to parasitic vibrations. However, the circuit is more complex, which necessitates a larger number of components because a gate driver is installed for each device. In the common method, only one driver is needed, but resonance between the gate wiring inductance and the input capacitance may occur, causing the MOSFETs to malfunction during switching. Therefore, as a means of preventing malfunctions, gate resistors and gate-source capacitances are connected to each device in order to suppress resonance.

Finally, with regard to the main circuit, the stray inductance L_s between each module and the direct-current link capacitor leads to a current imbalance, which causes differences in the losses of each device because the current is diverted by the ratio of L_s [6]. The current imbalance due to stray inductance in the main circuit has been discussed when implementing parallel drive of SiC MOS modules with high speed operation and high density [5] [6]. On the other hand, the effect of mutual inductanc e between the gate driver and the main circuit has not been discussed. This paper describes a method for optimizing parallel drives by clarifying the influence of mutual inductance between the gate driver and the main circuit and the stray inductance of the main circuit when parallel drive is performed using the 3.3-kV/800-A all-SiC MOSFET module in the iXPLV package developed by the company.

2 Construction of parallel-driven evaluation systems

2.1 Devices in use and evaluation circuits

Figs. 1 and 2 show the 3.3-kV/800-A all-SiC module in the iXPLV package developed by the company, which features low stray inductance and high-power density [7]. The basis of the evaluation circuit configuration in this paper is shown in Fig. 3. A common gate-drive system was used. V_{DD} represents the main voltage supply, C represents DC link capacitor, and L_m represents inductive loads. Gate resistors $R_{g1–4}$ and external gate-to-source capacitances $C_{gs1–4}$ were inserted at each gate. $L_{s1–4}$ represents the stray inductance of the main circuit and $M_{1,2}$ represents the mutual inductance of the stray inductance L_s of the main circuit and the external capacitance C_{gs}.

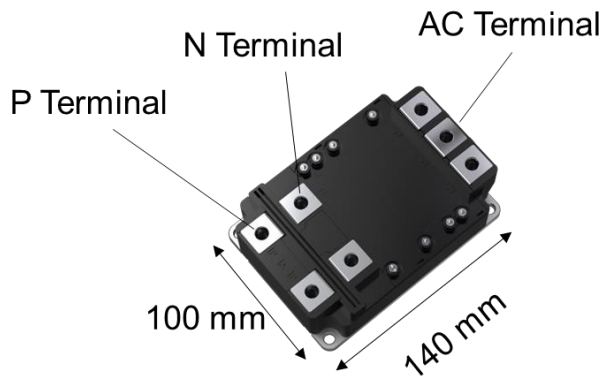


Fig. 1 3.3-kV/800-A, 2-in-1 all-SiC module (iXPLV).

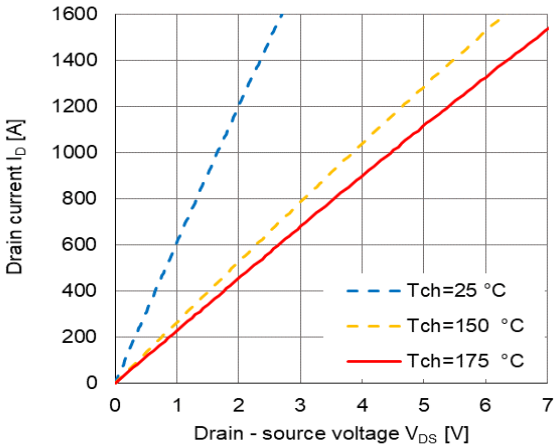


Fig. 2 Forward I_D-V_{DS} characteristics in the on-state (V_{gs} = +20 V) of the 3.3-kV/800-A, 2-in-1 all-SiC MOSFET module (iXPLV).

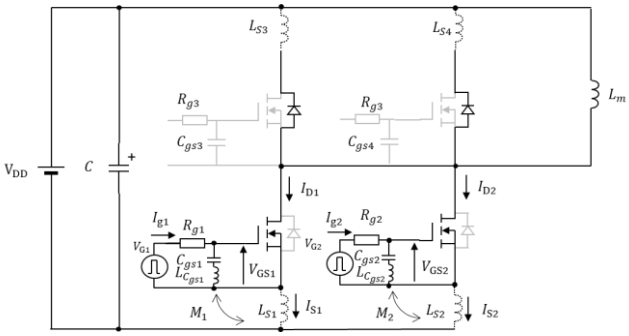


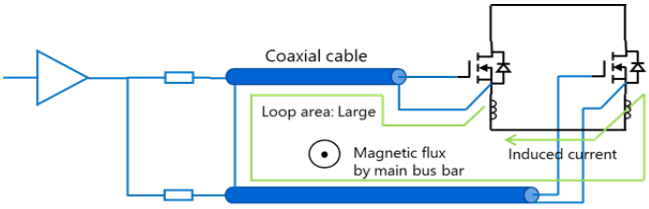
Fig. 3 Parallel drive evaluation circuit.

2.2 Influence of mutual inductance between gate wiring and main circuit

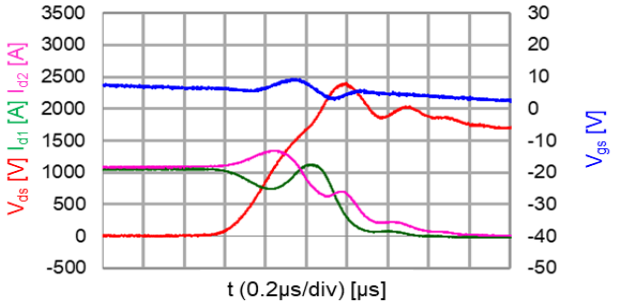
When devices to be driven in parallel are driven by a common gate driver, attention must be paid to the arrangement of the gate drive wiring. The effect of mutual inductance between the gate wiring and the main circuit was investigated using the evaluation circuit shown in Fig. 3. The measurement conditions were V_{DD}=1920 V, I_d=2300 A, $R_{g(on/off)}$=10 Ω/10 Ω, T_{ch}=175 °C, L_m=100 μH, $V_{GG(on/off)}$=+20 V/−6 V, C=1500 μF, C_{gs}=100 nF, and L_s=250 nH. The switching waveforms are shown in Fig. 4(b) when the gate wiring of each device is separated, as shown in Fig. 4(a). Large variations in V_{gs}, I_d, and V_{ds} were observed. This is because the area of the low-impedance loop due to the source line is larger, and when the magnetic flux due to the main circuit current penetrates this loop, current flows in the loop. As a result, the gate voltage fluctuates due to the resistance and inductance components, leading to device

breakdown. However, when the gate wiring is placed close together, as shown in Fig. 5(a), the V_{gs} fluctuations subside and improve, as shown in Fig. 5(b).

This is attributed to the gate wirings being close to each other and having a small loop area, which reduces the mutual inductance of the main circuits and thus reduces the gate voltage fluctuations due to magnetic flux. It is therefore important to keep the gate wirings of devices that are driven concurrently as close together as possible.

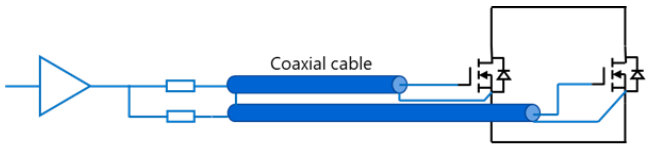


(a)

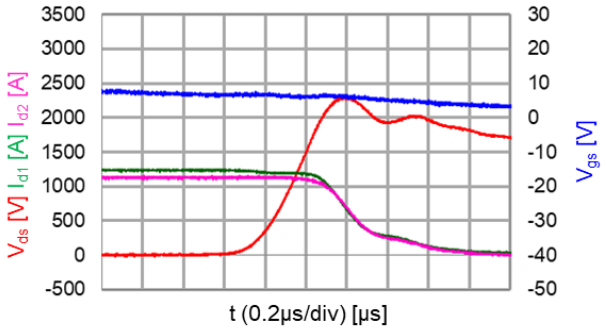


(b)

Fig. 4 Circuit concept diagram with gate wiring separated (a) and turn-off switching waveforms (b).



(a)



(b)

Fig. 5 Circuit concept with gate wiring in close proximity (a) and turn-off switching waveforms (b).

2.3 Influence of mutual inductance between the external gate-source capacitor and main circuit

In devices with fast switching capability, such as SiC MOSFETs, a capacitor may be connected between the gate and source in order to reduce gate noise. However, it is important to pay attention to the mutual induction between the inductance of the capacitor connection loop and the stray inductance of the main circuit. Devices such as SiC-MOSFETs that can operate at high speeds generate a back electromotive force due to mutual induction which causes the gate voltage to fluctuate. Equation (1) shows the gate voltage Vgs of the equivalent circuit in Fig 3.

$$V_{gs} = \frac{1}{C_{gs}} \int I_{c_{gs}}\, dt + \left(L_{cgs} \frac{dI_{C_{gs}}}{dt} + M \frac{dI_d}{dt} \right) \quad (1)$$

Where: $i_{c_{gs}}$ is current of C_{gs}.

From equation (1), as dI/dt increases due to high-speed operation, the effect of mutual inductance increases. This can result in unintended false turn-on during off state. To check the effect of switching due to mutual inductance with the external capacitor C_{gs}, simulations were performed using the LT Spice Simulator. Simulations were performed with the evaluation circuit simulating Fig. 3 and the measurement conditions V_{DD} = 1800 V, I_d = 800 A, $R_{g(off)}$ = 3.9 Ω, T_{ch} = 175 °C , $V_{GG(on/off)}$ = +20 V/−6 V, L_s = 70 nH, C_{gs} = 100 nF and L_{cgs} = 15 nH with a single drive. Fig. 6 shows the relationship between dI/dt when the mutual inductance M is varied. As the mutual inductance M shifts towards the positive side, dI/dt tends to become lower and switching loss increases. Meanwhile, dI/dt increases as the shift towards the negative side, and at M = −3 nH, the electromotive force due to mutual induction becomes significantly peaks sharply, as shown in Fig. 7.

Simulations were performed in parallel drives in order to investigate the effect of the difference between the mutual inductance M and the device threshold voltage V_{th} in parallel drives. The measurement were performed with two devices driven in parallel at I_D = 1600 A. Other conditions were the same as those for the single drive. If there is no difference in V_{th} and the mutual inductance is M = −3 nH, then the waveform will have two devices falsely turning-on simultaneously, as shown in Fig. 8. When there is a difference in V_{th}, as shown in Fig. 9, the switching timing shifts and the waveform repeats alternating falsely turning-on. This state is an overcurrent condition, given that the current should be shared by two devices, but is borne by one, which can lead to device breakdown. Therefore, in parallel drives, the influence of

the mutual inductance of the main circuit and C_{gs} is more pronounced, and the mounting method of the external C_{gs}, which determines the mutual inductance, must be fully considered.

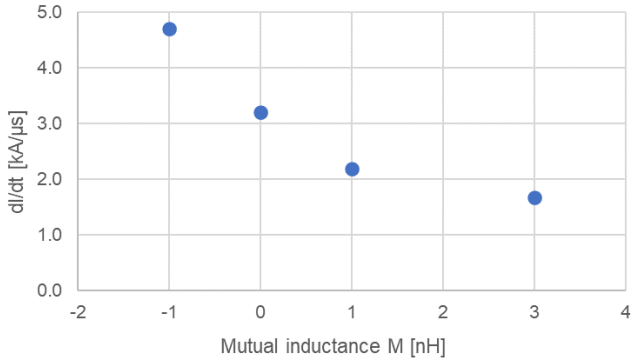


Fig. 6 Relationship between mutual inductance M and dI/dt.

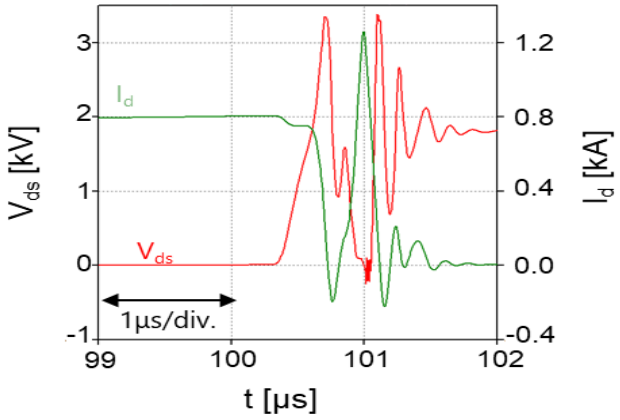


Fig. 7 Turn-off switching waveform at mutual inductance M = -3 nH in single operation.

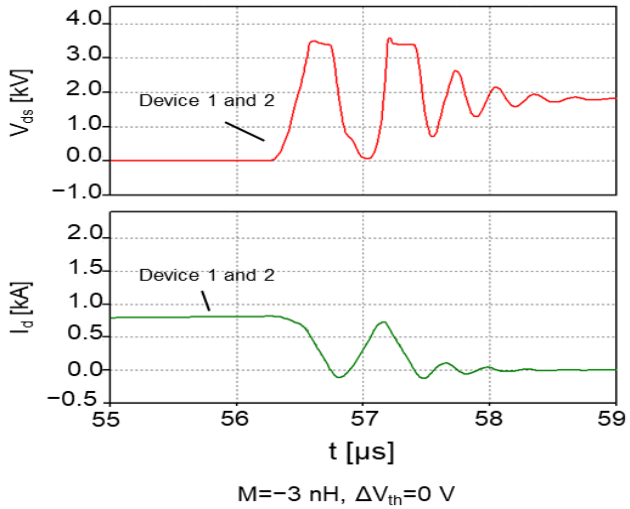


Fig. 8 Turn-off switching waveform at a threshold voltage difference of 0 V and mutual inductance M = −3 nH in parallel operation.

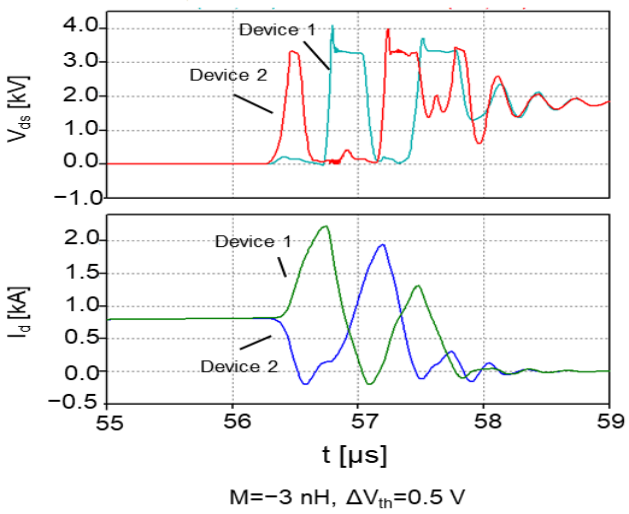


Fig. 9 Turn-off switching waveform at a threshold voltage difference of 0.5 V and mutual inductance M = −3 nH in parallel operation.

2.4 Influence of stray inductance in the main circuit

As discussed above, stray inductance in the main circuit causes current imbalance, which may lead to reliability degradation due to variations in device temperature. Attempting to align the inductance of the main circuit can increase the total inductance. The effect of increased inductance on switching was confirmed by simulation.

Fig. 10 shows the waveform results of the simulation of inductive load switching with a main circuit inductance of L_s = 70 nH and 140 nH under identical conditions. The measurement conditions were V_{DD}=1800 V, I_d=800 A, $R_{g(on)}/Rg_{(off)}$=2.2 Ω/3.9 Ω, T_{ch}=175°C, L_m=100 μH, $V_{GG(on/off)}$=+20 V/−6 V and $C_{gs1–4}$=100 nF. At turn-on, when L_s was large, the voltage dropped significantly due to di/dt caused by the rise in current.

Consequently, turn-on loss E_{on} became small, as shown in Fig. 11(a). In contrast, during turn-off, the energy stored in L_s generated a turn-off surge, which was proportional to L_s. As L_s increased, the turn-off loss E_{off} also increased, as shown in Fig. 11(b).

Fig. 12 shows the calculated loss for each device, assuming a two-level inverter, and confirms that they decreased as L_s increased. In contrast, the t urn-off surge increased as L_s increased. Therefore, it is important to design equal stray inductance, even if it increases the total inductance, in order to align the imbalanced current within the range where turn-off surge is acceptable.

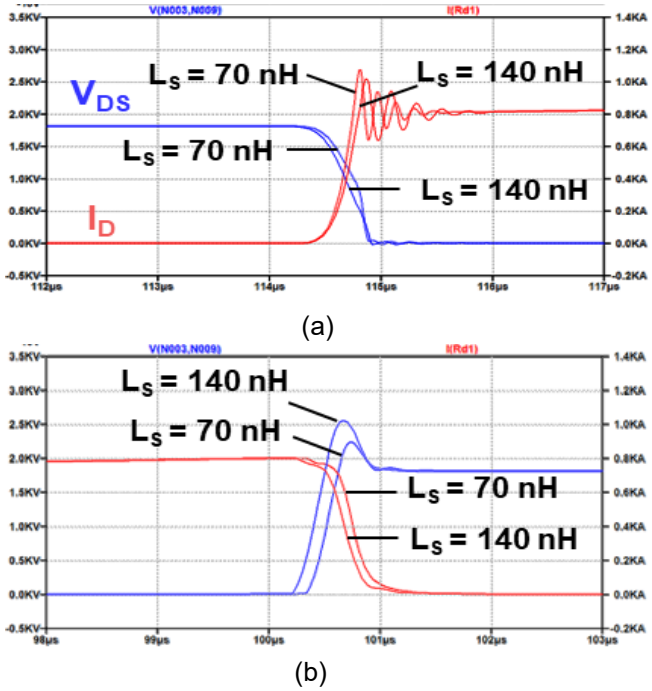


Fig. 10 (a) Turn-on and (b) turn-off waveform of the Inductive load switching simulation.

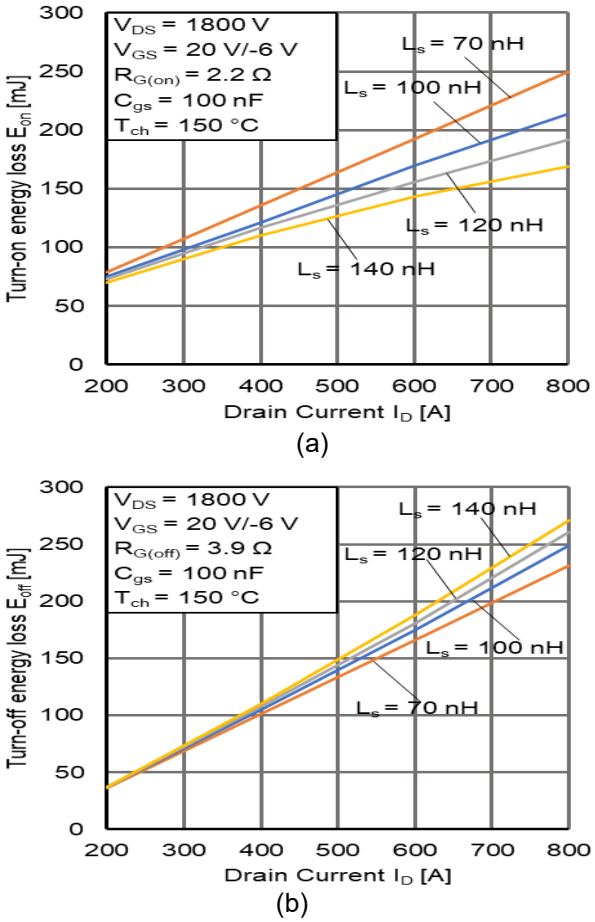
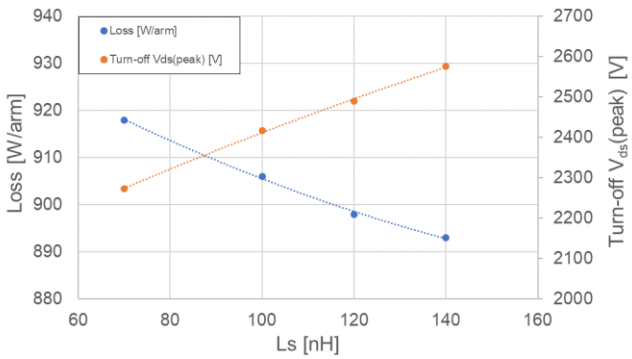


Fig. 11 Dependence of switching losses on stray inductance of busbar.



Loss calculation conditions: Two-level sinusoidal inverter, S_{out} = 1800 kVA, V_{DD} = 1800 V, V_{out} (line-to-line) = 1100 V, p.f. = 0.8, f_{sw} = 3 kHz, T_f = 100 °C

Fig. 12 Stray inductance dependence of loss and Turn-off V_{DS} (peak).

3 Evaluation of parallel drives on actual equipment

To demonstrate the influence of the mutual induction M between the external capacitance C_{gs} and the main circuit and the influence of the difference in stray inductance L_s of the main circuit, the circuit shown in Fig. 3 was constructed and evaluated in an actual machine. The gate wiring of each device connected to the gate drive circuit is as equidistant and as close as possible to the gate wiring of each device described in section 2.2.

As shown in Table 1, the devices to be driven in parallel are selected with the threshold voltage V_{th} and the on-voltage aligned. The evaluation circuit and device were used for switching evaluation by double-pulse testing under two conditions, as shown in Table 2.

The measurement conditions were V_{DD}=1800 V, I_d=1600 A, T_{ch}=175 °C, $R_{g(on)}/Rg_{(off)}$=1.5 Ω/3.6 Ω, $V_{GG(on/off)}$=+20 V/−6 V, L_m=100 µH and $C_{gs1–4}$ =100 nF. To check the effect of the external capacitors C_{gs}, lead-type capacitors were used in Condition 1 and chip-type capacitors were used in Condition 2.

The busbars connected to each device were designed differently in Conditions 1 and 2 in order to vary the stray inductance of the main circuit. Each busbar is made of Cu and is 1.0 mm thick. The structure of the P- and N-terminal busbars is shown in Fig. 12. The distance d between the busbars of the P and N terminals of Condition 2 is narrower than that in Condition 1, which has the effect of reducing the total stray inductance of the main circuit by causing the magnetic fluxes at the P and N terminals to cancel each other out.

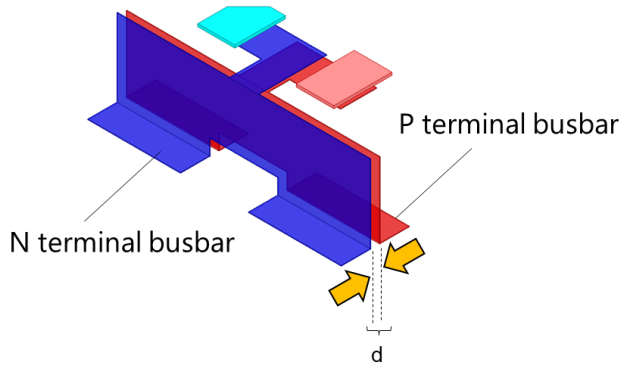
The busbars for the AC terminals are shown in Fig. 13. As shown in Fig. 13(a), Condition 1 was designed with a simple busbar of equal length, while Condition 2 was designed so that the AC terminals are of equal length from the load-connection point. This structure reduces the difference in stray inductance for each element in Condition 1 compared with Condition 2.

	V_{th} [V] T_{ch} = 175°C V_{ds} = 10 V I_d = 0.8 A	$V_{ds(on)}$ [V] T_{ch} = 175°C V_{gs} = 20 V I_d = 800 A
SiC MOSFET module 1	3.75	3.73
SiC MOSFET module 2	3.77	3.74
Δ	0.02	0.01

Table 1 Characteristics of devices to be driven in parallel.

	Condition 1	Condition 2
	Ls [nH]	Ls [nH]
SiC MOSFET module 1	120	97
SiC MOSFET module 2	151	105
Total Ls	67	50
ΔLs	31	8
External C_{gs} type	Lead	Chip

Table 2 Stray inductance and external gate-source capacitor types for Conditions 1 and 2.



	Condition 1	Condition 2
d (Ratio)	1	0.25

Fig. 12 Design of P and N terminal busbar for conditons1 and 2

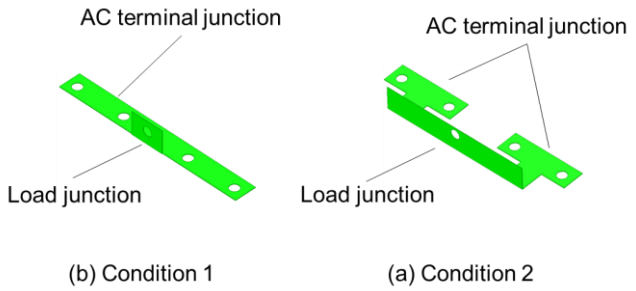


Fig. 13 Design of AC terminal busbars for Conditions 1 and 2.

Fig. 14 show the turn-off switching waveform for Condition 1, in which the difference in the steady-state on-state current imbalance at turn-off is 8%. This is thought to be due to the large difference in the main circuit Ls and the large steady-state unbalance. In turn-off, the difference in dI/dt is thought to be due to the large mutual inductance of the lead type C_{gs}.

Fig. 15 show the turn-off switching waveform of Condition 2, in which the current imbalance in the steady-state on-state of the two devices in parallel from the turn-on waveform is small, at about 1%. This is considered to be due to the small difference in the main circuit Ls, which results in a small steady-state unbalance. In addition, no difference in dI/dt can be seen between the devices. This is considered to be because the external C_{gs} is a chip type and the loop formed by the main circuit and C_{gs} is small and the mutual inductance with the main circuit is also small, so there is no difference in dI/dt. The slight shift during switching is considered to be due to a slight difference in the V_{th} of the device's high temperature.

Based on the measured switching waveforms, the losses and the average channel temperature difference were calculated assuming a two-level inverter. The losses are calculated per inverter arm and assume no load fluctuations. The results for the losses are shown in Fig. 16 and the results for the average channel temperature are presented in Table 3. For Condition 1, the temperature difference between the two devices is large at 9.6°C due to the large loss difference. For Conditon2, due to the small in difference loss, the average channel temperature difference between the two devices is small at 1.6°C. A large temperature difference between each device affects the life of the device [4] [8] [9]. Particularly in applications with large load fluctuations, such as railway applications, there are failure modes such as bonding wires being subjected to stress and breaking as the device temperature rises and falls. It is important to adjust the current imbalance by aligning

the stray inductances of each device because differences in device life may result in a shorter-than-expected lifetime for the entire system.

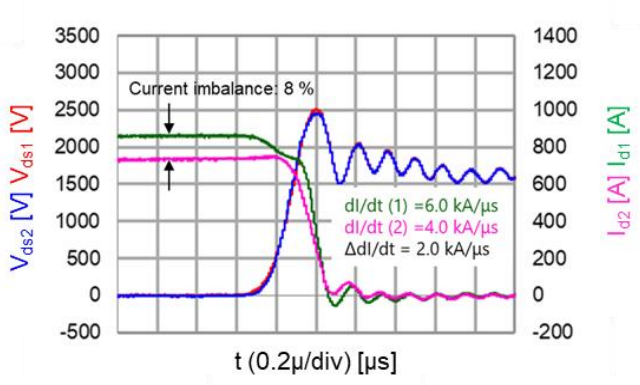


Fig. 14 Turn-off switching waveforms for Condition 1.

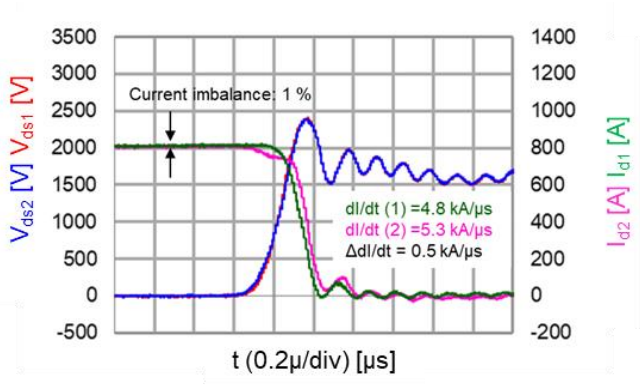
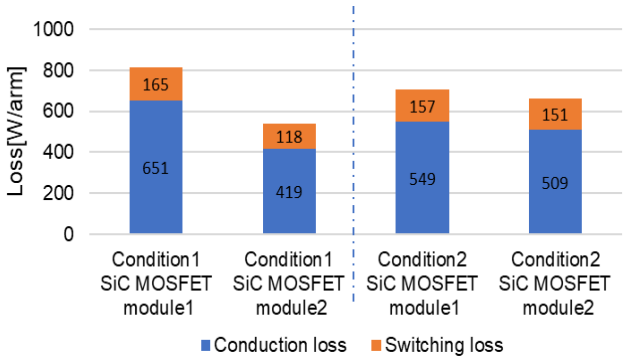


Fig. 15 Turn-off switching waveforms for Condition 2.



Loss calculation conditions: two-level sinusoidal inverter, S_{out} = 1800 kVA, V_{DD} = 1800 V, V_{out} (line-to-line) = 1100 V, p.f. = 0.8, f_{sw} = 3 kHz, T_f = 100°C

Fig. 16 Two-level inverter loss simulation results based on switching waveform measurements for Conditions 1 and 2.

	Condition 1		Condition 2	
	SiC MOSFET module 1	SiC MOSFET module 2	SiC MOSFET module 1	SiC MOSFET module 2
T_{ch} [°C]	128.2	118.6	124.4	122.8
ΔT_{ch} [°C]	9.6		1.6	

Table 3 Average channel temperatures for each device and the difference between them when two-level inverters are used.

4 Conclusion

When implementing parallel drives using SiC MOS modules, which can be densified and operated at high speed, the effects of mutual inductance in the gate driver and main circuit and the effects of current imbalance due to stray inductance in the main circuit were identified and the optimum method was described.

The influence of mutual inductance between the gate driver and the main circuit lies in the low impedance loop of the gate wiring, and it is important to make the gate wirings close to each other to reduce the low impedance loop.

When an external capacitor C_{gs} is inserted as a gate noise countermeasure, the mutual inductance between the main circuit and C_{gs} can be reduced by making the loop between the main circuit and C_{gs} smaller. As a result, there is no difference in dI/dt and the timing is less likely to shift.

The difference in stray inductance of each device in the main circuit causes a current imbalance, resulting in differences in the losses of each device. This results in a difference in the thermal fatigue life of each device, which shortens the expected life of the system. It is therefore important to match stray inductances of the main circuits within the range where turn-off surges are allowed. The above results demonstrate the most effective method for driving SiC MOSFET modules in parallel.

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